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MS-7581

ATX

Ver: 0B

CPU:

INTEL -HAVENDALE/Lynnfied LGA 1156

System Chipset:

INTEL-IBEXPEAK PCH

OnBoard Chipset:

Clock Gen:IDT 4100

HD Audio Codec:RTL889

LAN:Intel integrated Hanksville 10/100/1000 NIC

SIO:FIN71889

Flash ROM: 32 Mb SPI (CHIP)

Main Memory:

DDRIII (1066/1333MHz) * 4 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X8) Slot * 1

PCI Express (X1) Slot * 1

PCI Slot * 1

PWM:

Controller:ISL6334 (4-Phase 95W)

Controller:ISL

ACPI:

INTERSIL

Other:

SATA(SATA2-300MB/s) *4

USB2.0 *14 (Rear*6 Front*4 Intrenal *4)


DISPLAY PORT*1

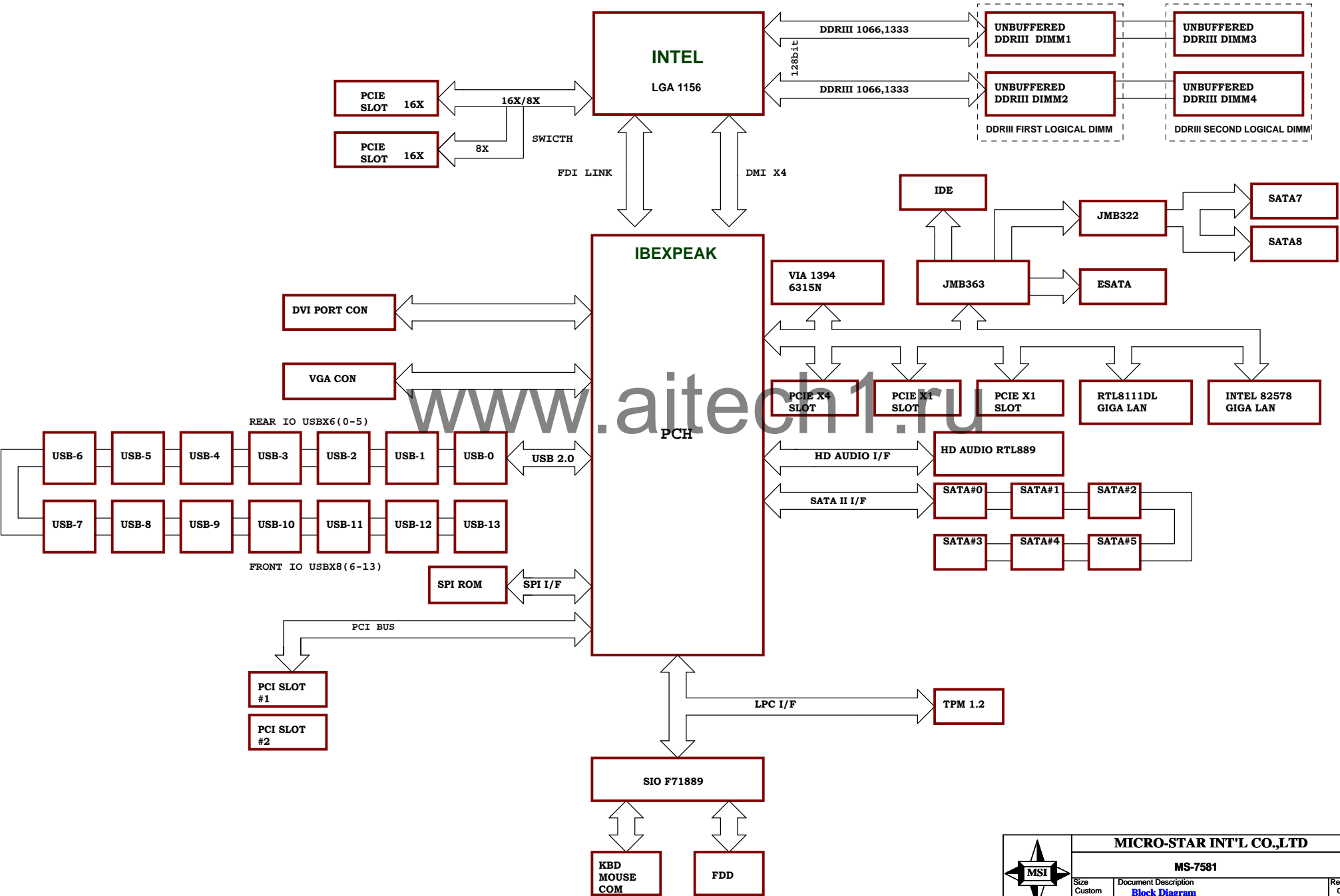
VGA PORT *1

PRINT Header *1

COM PORT *1

COM Header *1

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DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 2 CH-A	10100000B	MEM_MAO_CLK_H0/L0 MEM_MAO_CLK_H1/L1 MEM_MAO_CLK_H2/L2
DIMM 4 CH-A	10100010B	MEM_MA1_CLK_H0/L0 MEM_MA1_CLK_H1/L1 MEM_MA1_CLK_H2/L2
DIMM 1 CH-B	10100001B	MEM_MBO_CLK_H0/L0 MEM_MBO_CLK_H1/L1 MEM_MBO_CLK_H2/L2
DIMM 3 CH-B	10100011B	MEM_MB1_CLK_H0/L0 MEM_MB1_CLK_H1/L1 MEM_MB1_CLK_H2/L2

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INT#E PCI_INT#F PCI_INT#G PCI_INT#H	PCI_REQ0# PCI_GNT0#	AD16	CLK33M_PCISLOT_J20
TPM				LPCCLK0
SIO				LPCCLK1

TABLE 9-1
USB PORT MAPPING (SUBJECT TO CHANGE)

Controller	Port	Destination	Fused	ESD Pads	Bulk Cap	Over-Current Detection
UHCI #1, EHCI #1	Port 0	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
	Port 1	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
UHCI #2, EHCI #1	Port 2	Internal (Media Reader - P150)	Yes	Yes	No	Yes
	Port 3	Internal (Media Reader - P150)	Yes	Yes	No	Yes
UHCI #3, EHCI #1	Port 4	Front I/O	Yes	Yes	No	Yes
	Port 5	Front I/O	Yes	Yes	No	Yes
UHCI #4, EHCI #2	Port 6	Front I/O	Yes	Yes	Yes	Yes
	Port 7	Front I/O	Yes	Yes	Yes	Yes
UHCI #5, EHCI #2	Port 8	Rear I/O	Yes	Yes	Yes	Yes
	Port 9	Rear I/O	Yes	Yes	Yes	Yes
UHCI #6, EHCI #2	Port 10	Rear I/O	Yes	Yes	Yes	Yes
	Port 11	Rear I/O	Yes	Yes	Yes	Yes
UHCI #7, EHCI #2	Port 12	Rear I/O	Yes	Yes	Yes	Yes
	Port 13	Rear I/O	Yes	Yes	Yes	Yes

PCI RESET DEVICE

IBEXPEAK	
Signals	Target
PCIRST#	PCISLOT1
PE_RST#	TPM_RST#
PE_RST#	LPC/SIO




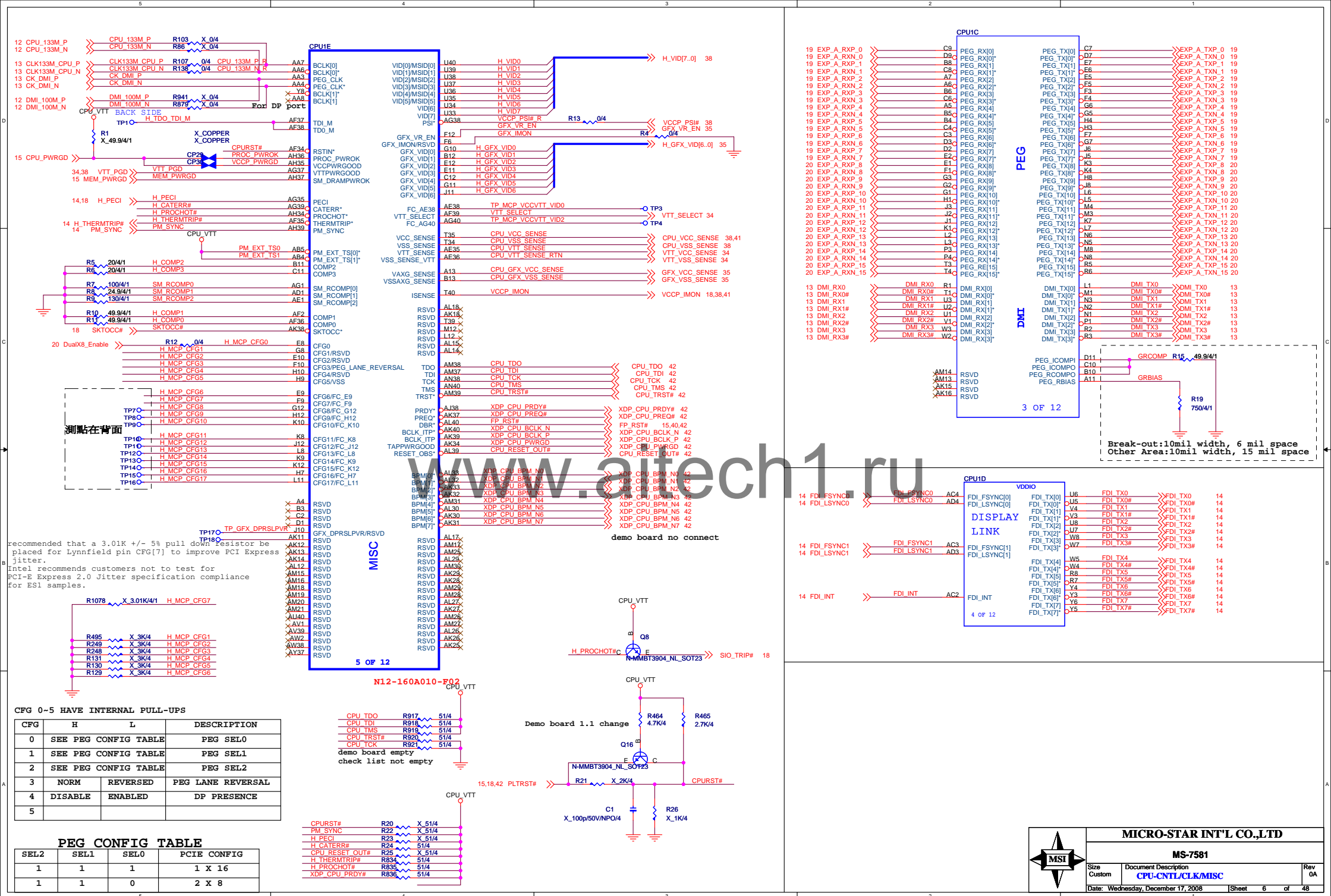
IBEXPEAK GPIO DEFINITION									
Pin	GPIO	POWER WELL	IO	Function	Implementation	Function			
AK41	GPIO0	MAIN	I	BMBSU#	Pull-up to +3.3V and connect to the PECL_REQ# pin (TBD) on the SIO.	PECL_REQ#			
AL14	GPIO1	MAIN	I	IACH1	Through a 0Ω series resistor, connect to one of the front fan's TACH interface circuit.	IACH1			
AU8	GPIO2	MAIN	I	PCI_IRQ#	See PCA Spec	PCI Interrupt E#			
AH7	GPIO3	MAIN	I	PCI_IRQ#	See PCA Spec	PCI Interrupt F#			
AP12	GPIO4	MAIN	I	PCI_IRQ#	See PCA Spec	PCI Interrupt G#			
AW4	GPIO5	MAIN	I	PCI_IRQ#	See PCA Spec	PCI Interrupt H#			
AY11	GPIO6	MAIN	I	IACH2	Pull-up to +3.3V and connect to P52 pin 12. The COMM_B assembly connects pin 12 directly to GND.	COMM_B_DET#			
AY11	GPIO7	MAIN	I	IACH3	Through a 0Ω series resistor, connect to one of the front fan's TACH interface circuit.	IACH3			
AK30	GPIO8	RESUME	O	IOG_EN#		Reserved			
AL28	GPIO9	RESUME	I	OC5	Associated with USB port05 powerwell. For ICH debug purposes, each USB_OC# signal must be accessible for probing.	USB_OC#			
AL30	GPIO10	RESUME	I	OC6	Pull-up to +3.3VSB and pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_ID2			
AL31	GPIO11	RESUME	I	SMBALERT#	Pull-up to +3.3VSB. It is always enabled as a wake event.	SMBALERT#			
AU34	GPIO12	RESUME	I	LAN_DISABLE	Follow implementation in Intel Picton Design Guide	LAN_DISABLE#			
AR16	GPIO13	RESUME	I	IO_PME	Pull-up to +3.3V SB and connect to P151-pin 10; also add a no-installed pulldown to the net.	RDYBST_DET#			
AM30	GPIO14	RESUME	I	OC7	Pull-up to +3.3VSB and connect to the SMI pin on the SIO.	DASH_SMI			
AY36	GPIO15	RESUME	I	PCH_GP15		SMI# from SIO			
AM39	GPIO16	RESUME	O	SATA4CP	Follow implementation in Intel Picton Design Guide	Reserved			
AW11	GPIO17	MAIN	I	IACH0	Through a 0Ω series resistor, connect to one of the front fan's TACH interface circuit.	CPU_MISSING			
AM39	GPIO18	MAIN	I	PCCLKRQ1#	Through a 1KΩ series resistor, pull-up to +3.3V and connect to E15-pin 1.	TACH0			
AM38	GPIO19	MAIN	I	SATA1CP	Pull-up to +3.3V and pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BOOT_BLK_REC#			
AP38	GPIO20	MAIN	I	PCCLKRQ2#		BRD_ID1			
AP37	GPIO21	MAIN	I	SATA0CP	Pull-up to +3.3V and connect to P23-pin 4.	PCIECLKRQ2#			
AN41	GPIO22	MAIN	I	SCLOCK	Pull-up to +3.3V and connect to P150-pin 10	FRNT_AUD_DET#			
AP14	GPIO23	MAIN	I	LDRQ1#	Pull-up to +3.3V and connect to the PCI SLOT Riser Detect circuit.	INT_USB_DET#			
AR34	GPIO24	RESUME	O	MEMLED	Through a 1kΩ series resistor, pull-up to +3.3VSB and connect to P125-Pin 1	RISER_DET#			
AP33	GPIO25	RESUME	I	PCIECLKRQ3#		HOOD_SW_DET#			
AW37	GPIO26	RESUME	I	PCIECLKRQ4#		PCIECLKRQ3#			
AP37	GPIO27	RESUME	O	OD_PLL_VR_EN		PCIECLKRQ4#			
AY40	GPIO28	RESUME	O	PCH_GP28		Reserved			
BA35	GPIO29	RESUME	O	SLP_LAN#	Connect to a circuit used to force the 3.3V_CL rail on.	WOL_EN			
AT37	GPIO30	RESUME	I	SUS_PWR_ACK					
AP40	GPIO31	MAIN	I	ACPRESENT	TBD. For now connect to a Test Point	ESATA_DET#			
AL40	GPIO32	MAIN	O	PCH_GP32	Through a 1kΩ series resistor, pull-up to +3.3V and connect to P1-pin 20.	85%_PS_DET#			
AT16	GPIO33	MAIN	O	PCH_GP33	Through a 1kΩ series resistor, pull-up to +3.3V and connect to pin 1 of Jumper E1.	FDT_OVRD#			
AT40	GPIO34	MAIN	O	SP_PCH	Pull-down to GND and connect to P124-pin 2. Decouple with 0.1μF	HOOD_LOCK_DET			
AR41	GPIO35	MAIN	O	SATACLKREQ#	Pull-up to +3.3V and connect to top-layer ring of PCA mounting hole used for SMT Baseband detect feature.	BRD_REV0			
AK39	GPIO36	MAIN	I	SATA2CP	Pull-up to +3.3V and pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_REV1			
AR38	GPIO37	MAIN	I	SATA3CP	Pull-up to +3.3V and connect to P126-pin 16	PRNTR_DET#			
AM38	GPIO38	MAIN	I	SLOAD	Through a series 1K resistor, connect to P5-pin 9 and pull-up to +3.3V	CHASSIS_ID0			
AL39	GPIO39	MAIN	I	SATA0OUT1	Pull-up to +3.3V and connect to top-layer ring of PCA mounting hole used for SMT Baseband detect feature.	BASEBAND_DET			
AT30	GPIO40	RESUME	I	OC1	Using an 8.2kΩ resistor, pull-down to GND and connect to E46-pin 2	PASSWDRD_EN			
AK28	GPIO41	RESUME	I	OC2	Associated with USB port2 powerwell. For ICH debug purposes, each USB_OC# signal must be accessible for probing.	USB_OC#			
AP30	GPIO42	RESUME	I	OC3	Associated with USB port3 powerwell. For ICH debug purposes, each USB_OC# signal must be accessible for probing.	USB_OC#			
AP31	GPIO43	RESUME	I	OC4	Associated with USB port4 powerwell. For ICH debug purposes, each USB_OC# signal must be accessible for probing.	USB_OC#			
AW38	GPIO44	RESUME	I	PCIECLKRQ5#		PCIECLKRQ5#			
AY36	GPIO45	RESUME	I	PCIECLKRQ6#		PCIECLKRQ6#			
AP36	GPIO46	RESUME	I	PCIECLKRQ7#		PCIECLKRQ7#			
AY39	GPIO47	RESUME	I	PEG_A_CLKRQ#		PEG_A_CLKRQ#			
AC38	GPIO48	MAIN	I	SATA0OUT1	Pull-up to +3.3V and connect to P24-pin 10	FRONT_USB_DET#			
AC40	GPIO49	MAIN	O	SATA3CP	Pull-up to +3.3V and pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_ID0			
AW35	GPIO50	MAIN	I	PCI_REQ1#	Use as REQ1#.	REQ1#			
AY35	GPIO51	MAIN	O	PCI_GNT1#	Use as GNT1#.	GNT1#			
AY34	GPIO52	MAIN	I	PCI_REQ2	Pull-up to +3.3V	REQ2#			
BA39	GPIO53	MAIN	O	PCI_GNT2	Connect to TP	GNT2#			
AM38	GPIO54	MAIN	I	PCI_REQ3	Through a 8.2kΩ series resistor, connect to P14-pin 2 and pull-down to GND.	BOOT_BLK_EN#			
AM35	GPIO55	MAIN	O	PCI_GNT3		GNT3#			
AW35	GPIO56	RESUME	I	PEG_B_CLKRQ#	Connect to circuit that controls the amplifier's output.	AUD_AMP_DIS#			
AL32	GPIO57	MAIN	I	PCH_GP57	Pull-up to +3.3VSB.	TPM_PP			
AY31	GPIO58	RESUME	O	SML1CLK		SML1CLK			
AD31	GPIO59	RESUME	I	OC8	Associated with USB port0 powerwell. For ICH debug purposes, each USB_OC# signal must be accessible for probing.	USB_OC#			
BA33	GPIO60	RESUME	O	SMDALERT#		SMDALARM			
AK31	GPIO61	RESUME	O	SUS_STAT#	Power Down for external TPM	LPCPD#			
AM31	GPIO62	RESUME	O	SUSCLK	SUSCLK to SIO	SUSCLK			
AU36	GPIO63	RESUME	O	SLP_S5#	Connect to USB Power Control on SIO	SLP_S5#			
AD10	GPIO64	MAIN	O	CLKOUTFLEX0		CLKOUTFLEX0			
AK1	GPIO65	MAIN	O	CLKOUTFLEX1		CLKOUTFLEX1			
AB6	GPIO66	MAIN	O	CLKOUTFLEX2		CLKOUTFLEX2			
AL3	GPIO67	MAIN	O	CLKOUTFLEX3		CLKOUTFLEX3			
AY34	GPIO72	RESUME	I	PCH_GP72	Through a series 1KΩ resistor, pull-up to +3.3VSB and connect to P5-pin 10.	CHASSIS_ID1			
AN35	GPIO73	RESUME	I	PCIECLKRQ0#		PCIECLKRQ0#			
AY32	GPIO74	RESUME	O	SML1ALERT#		SML1ALERT#			
AR31	GPIO75	RESUME	O	SML1DATA		SML1DATA			

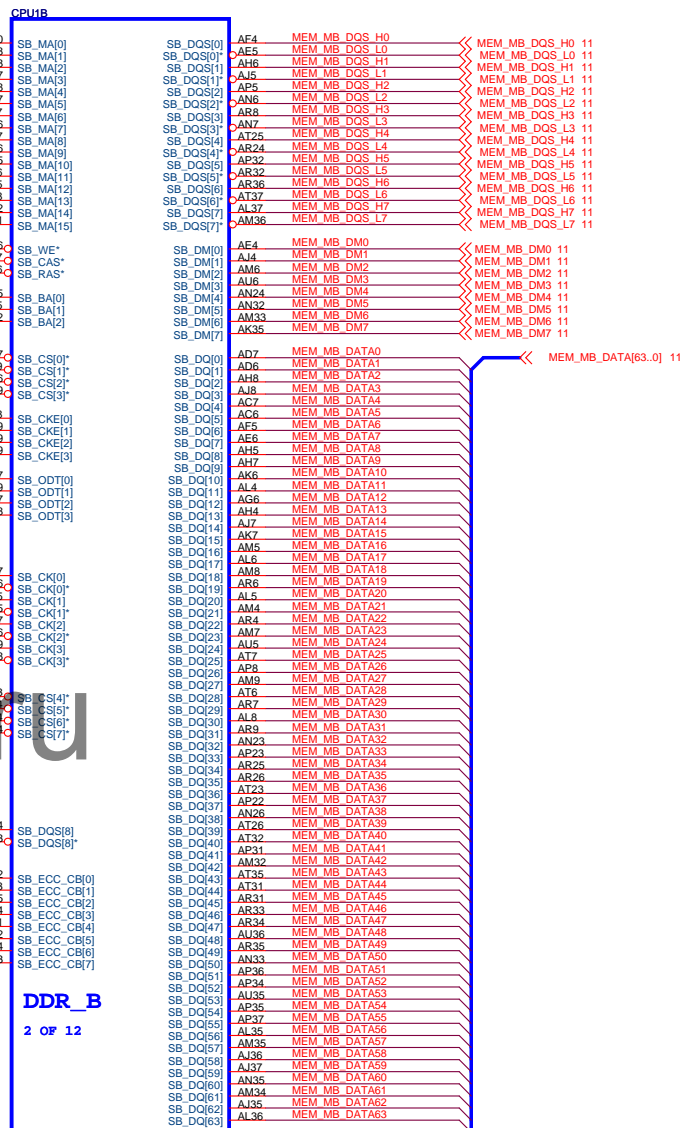
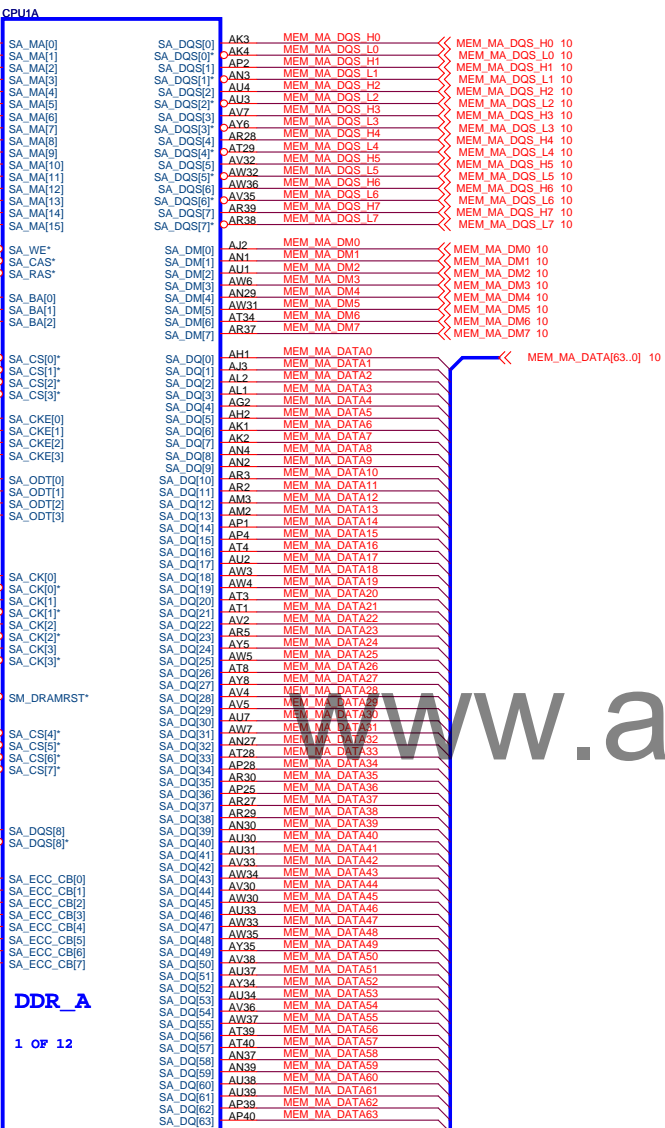
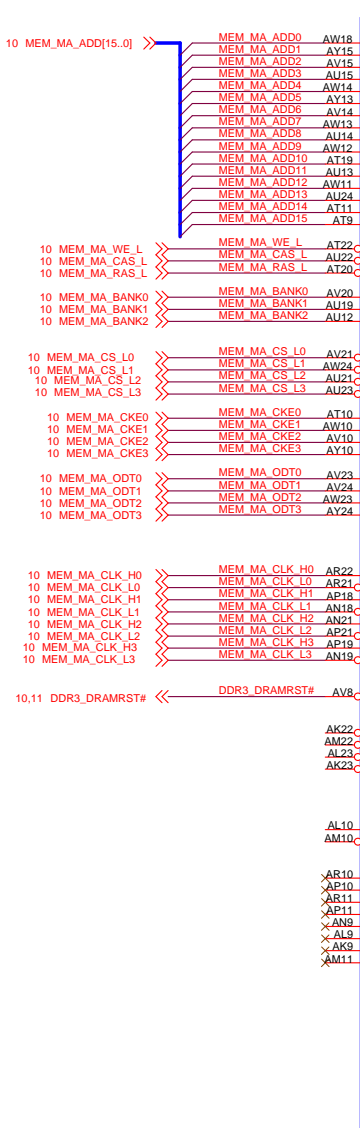
SIO9 PIN ASSIGNMENT (UPDATE PENDING)			
Pin	Pin Name	Function	Implementation
1	PWBTN#	PWRBTN#	Connect to front panel header's power button pin
2	SLP_S3#	SLP_S3#	Connect to ICH10's SLP_S3# signal
3	SLP_S5#	S4_STATE#	Connect to ICH10's S4_STATE# signal
7	PDS_EN	CPU_FAN_TACH	Connect to the CPU fan tach interface
8	COLOR	LED_PWR_COLOR	Controls the Power LED color
10	PWBTOUT#	PWRBTN_OUT#	Connect to ICH PWRBTN# input
11	PS_ON#	PS_ON#	Connect to the appropriate power supply circuit
13	BLINK_GR	LED_PWR_BLINK	Connect to PS.2 through 68 ohm series resistor.
14	SKOPME#	RING#	Connect to ICH8 R#
17	CLAMP_CTRL	CLAMP_CNTL	Use for clamping PCA voltage rails to decrease rail decay time
28	SMBISCL	SMB_CLK_MAIN	Connect to the clock signal of the main powered system SMBus
29	SMB2SCL	SMB_CLK_STDBY	Connect to the clock signal of the standby powered system SMBus
33	GPRSTZ#	PCI_EXP_RST#	Use to reset all the PCIe devices and slots
34	FANPWM2	CHAS_FAN_PWM	Connect to the Chassis Fan PWM interface
35	GPIO25	PWM_IN	Connect to the ICH10's PWM0 output - NEW for Eaglelake
36	PME_IN#	P_PME#	Connect to the PME# pin of the ICH10
37	USB_PWR#	USB_PWR#	Input to USB Power control; connect to the ICH10's SLP_S5# signal
38	3V_SW_MAIN#	3V_DUAL_CNTL	Connect to control inputs of dual rail switches
39	EVENT#	PCI_EXP_WAKE#	Connect to WAKE# pins of PCIe devices and slots
47	PDS_EN2	PDS_EN2	Use as control signal for appropriate voltage regulators
48	CPU_PRSTN1#	SKTOCC#	Connect to SKTOCC# on CPU
49	WAKE_OUT#	ICH_WAKE#	Connect to the ICH10's WAKE# input
50	GPIO14	HOOD_LOCK#	Connect to P124 pin 1 and a 2.2K pull-up to +5V.
51	GPIO16	HOOD_UNLOCK#	Connect to P124 pin 6 and a 2.2K pull-up to +5V.
53	AUDIO_BEEP	DIAG_BEEP	Connect to the system's integrated audio solution
54	FANPWM1	CPU_FAN_PWM	Connect to the CPU fan's PWM circuit
55	GPIO35	PECL_REQ#	Connect to the ICH10's BM_BUSY# signal - New for Eaglelake; C#/C4 support.
56	HD_LED_IN#	SATA_LED#	Connect to the ICH10's SATA_LED# output signal
58	HMSCL	HLTH_MON_CLK	Connect to CLK pin on SensorBus device
59	HMSDA	HLTH_MON_DAT	Connect to DAT pin on SensorBus device
60	GPIO10	FLPY_DRVEN	Use in floppy implementation
61	HD_LED_OUT#	HD_LED#	Connect to the front panel HDD LED
100	SMBYSDA	SMB_DATA_MAIN	Connect to the data signal of the main powered system SMBus
101	SMB2SDA	SMB_DATA_STDBY	Connect to the data signal of the standby powered system SMBus
102	5V_USB_MAIN#	5V_USB_MAIN#	Connect to the control pin of the 5V_DUAL circuit.
103	GPIO41	PS_FAN_TACH	Where applicable, connect to power supply's fan tach circuit.
104	FANPWM3	PS_FAN_PWM	Where applicable, connect to the power supply's fan PWM circuit
105	PWRGD_01	PWRGD_30MS	Use for appropriate system board sequencing
106	PWRGD_02#	PWRGD_30MS#	Use for appropriate system board sequencing
110	FAN_TACH4	CHAS_FAN_TACH	For systems with a chassis fan, connect to the chassis fan TACH circuit
111	SM1#	LPC_SM1#	Connect to appropriate ICH10 SMI-capable GPIO, reference ICH10 GPIO matrix
120	R12#	R12#	Where applicable, connect to appropriate serial port pin
122	DCD2#	DCD2#	Where applicable, connect to appropriate serial port pin
123	SIN2	SIN2	Where applicable, connect to appropriate serial port pin
124	SOUT2	SOUT2	Where applicable, connect to appropriate serial port pin
125	DSR2#	DSR2#	Where applicable, connect to appropriate serial port pin
126	RTS2#	RTS2#	Where applicable, connect to appropriate serial port pin
127	CTS2#	CTS2#	Where applicable, connect to appropriate serial port pin
128	DTR_BOUT2#	DTR2#	Where applicable, connect to appropriate serial port pin



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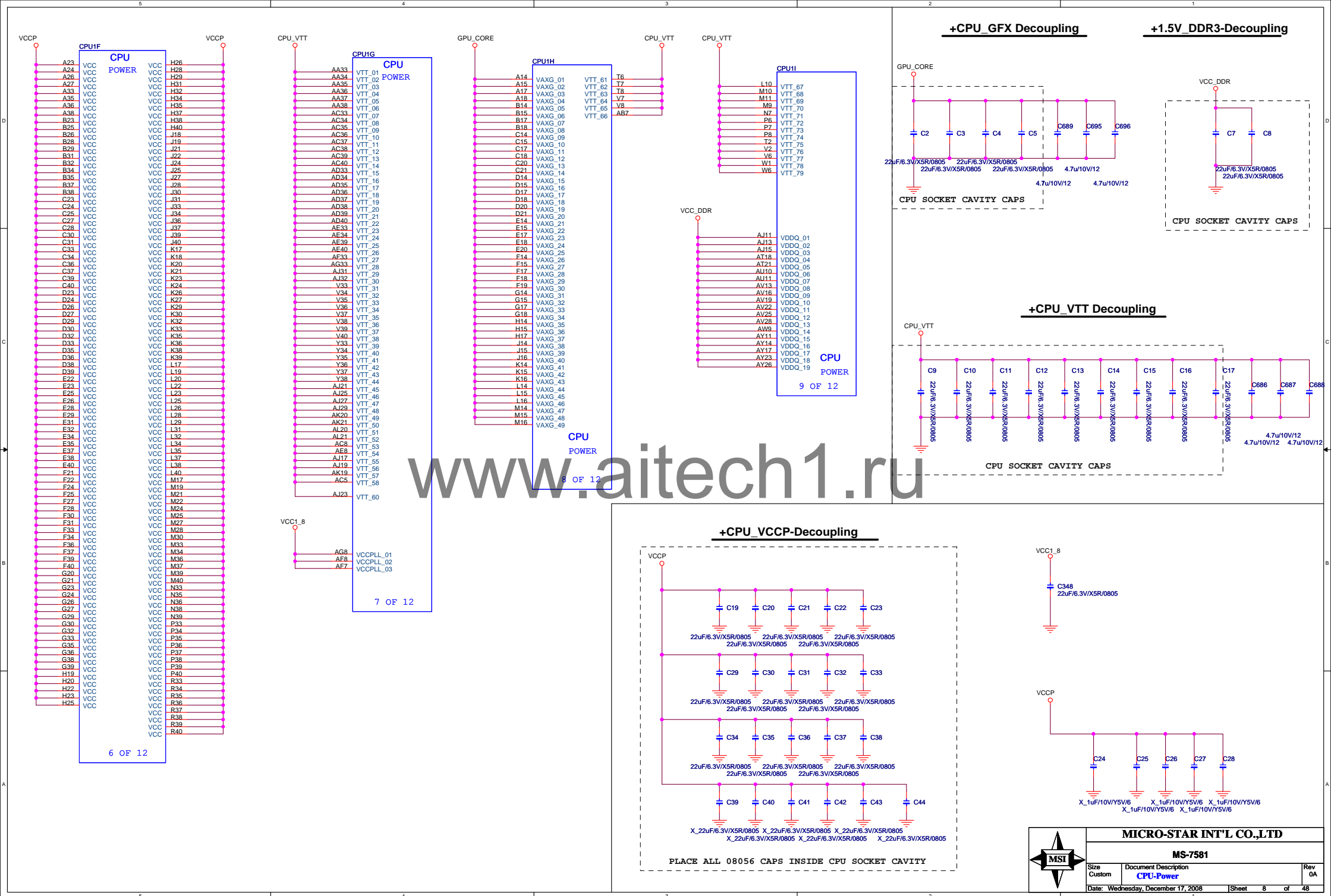




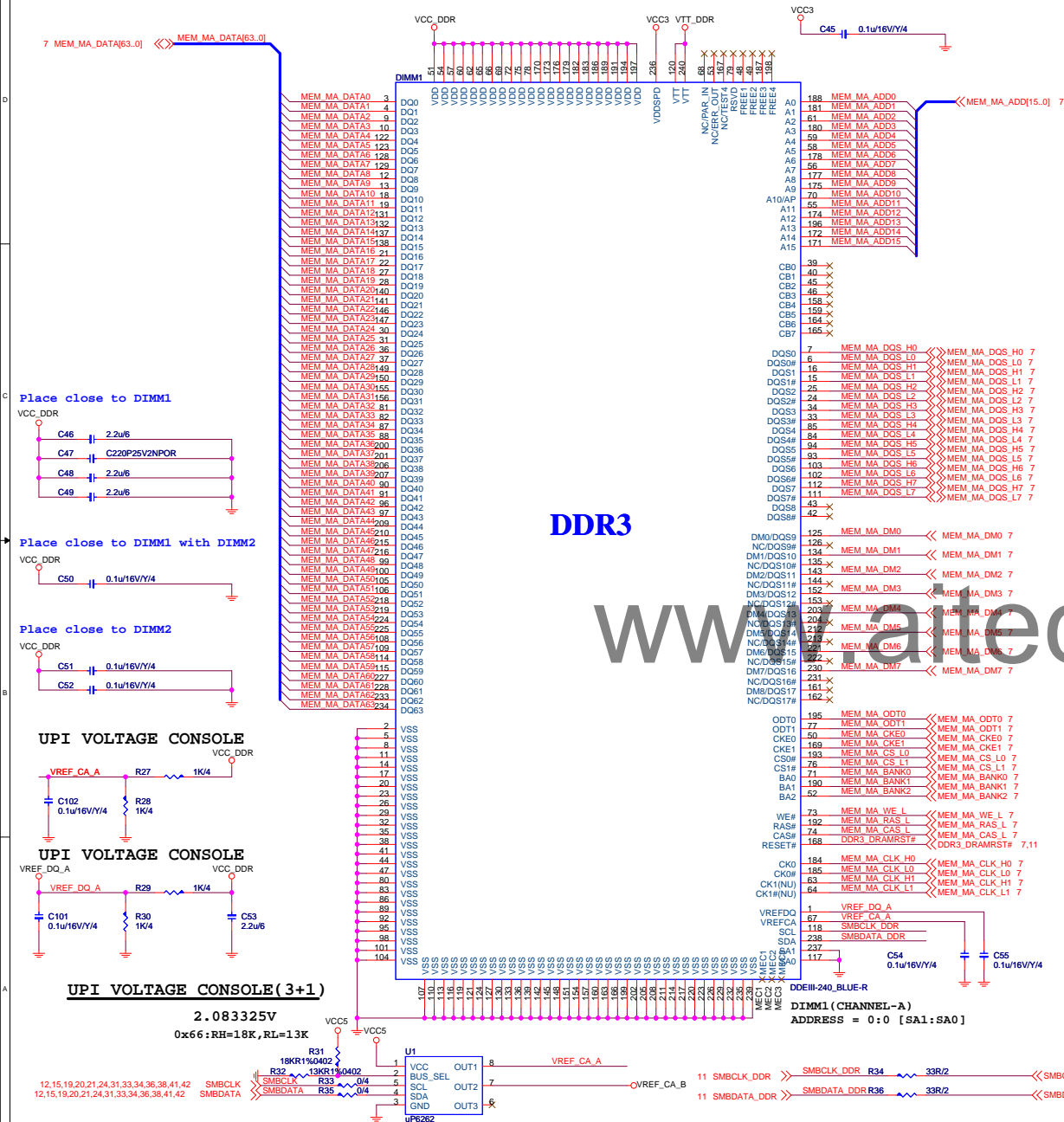
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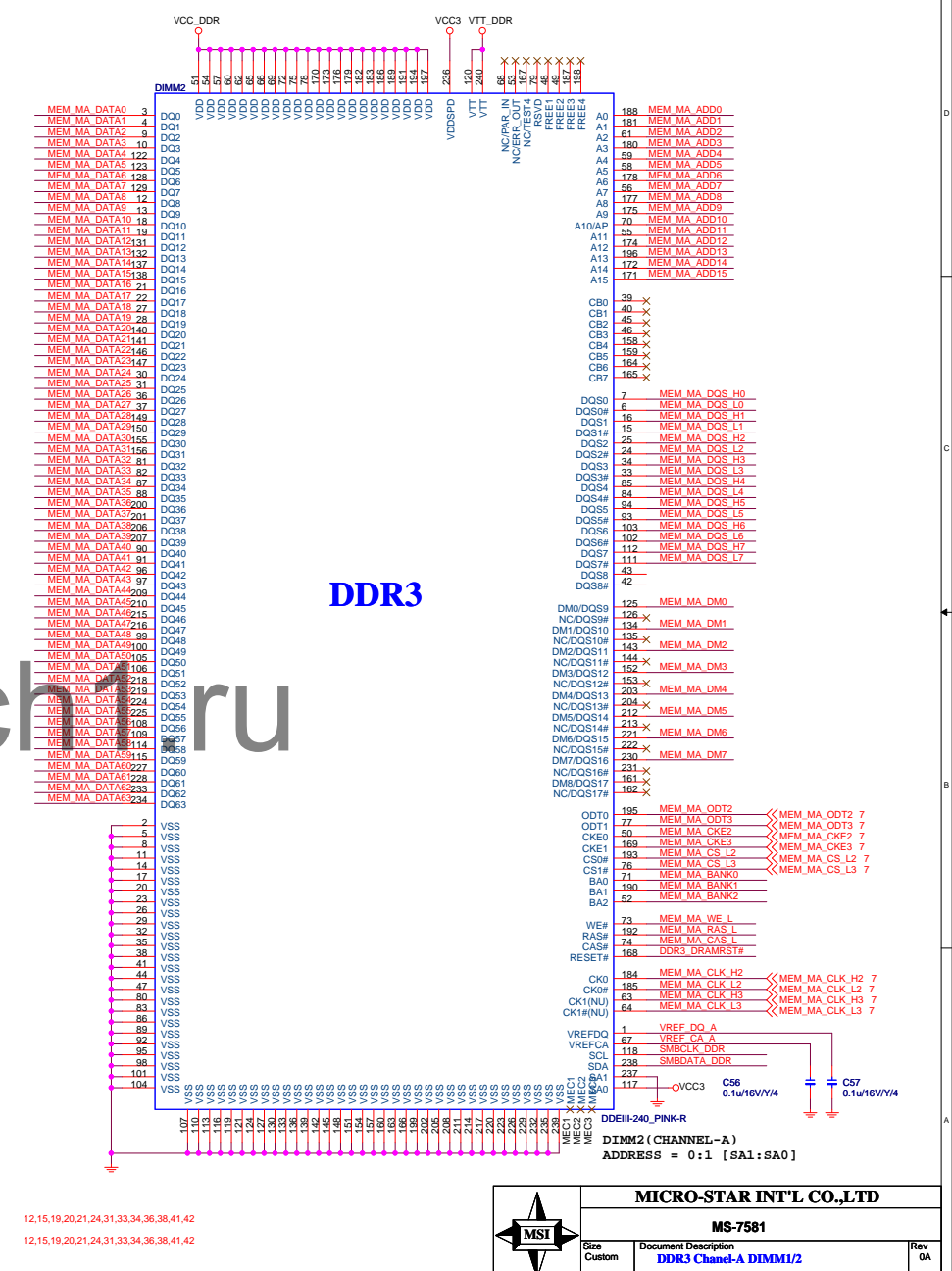
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DDRIII DIMM_A1



DDRIII DIMM_A2



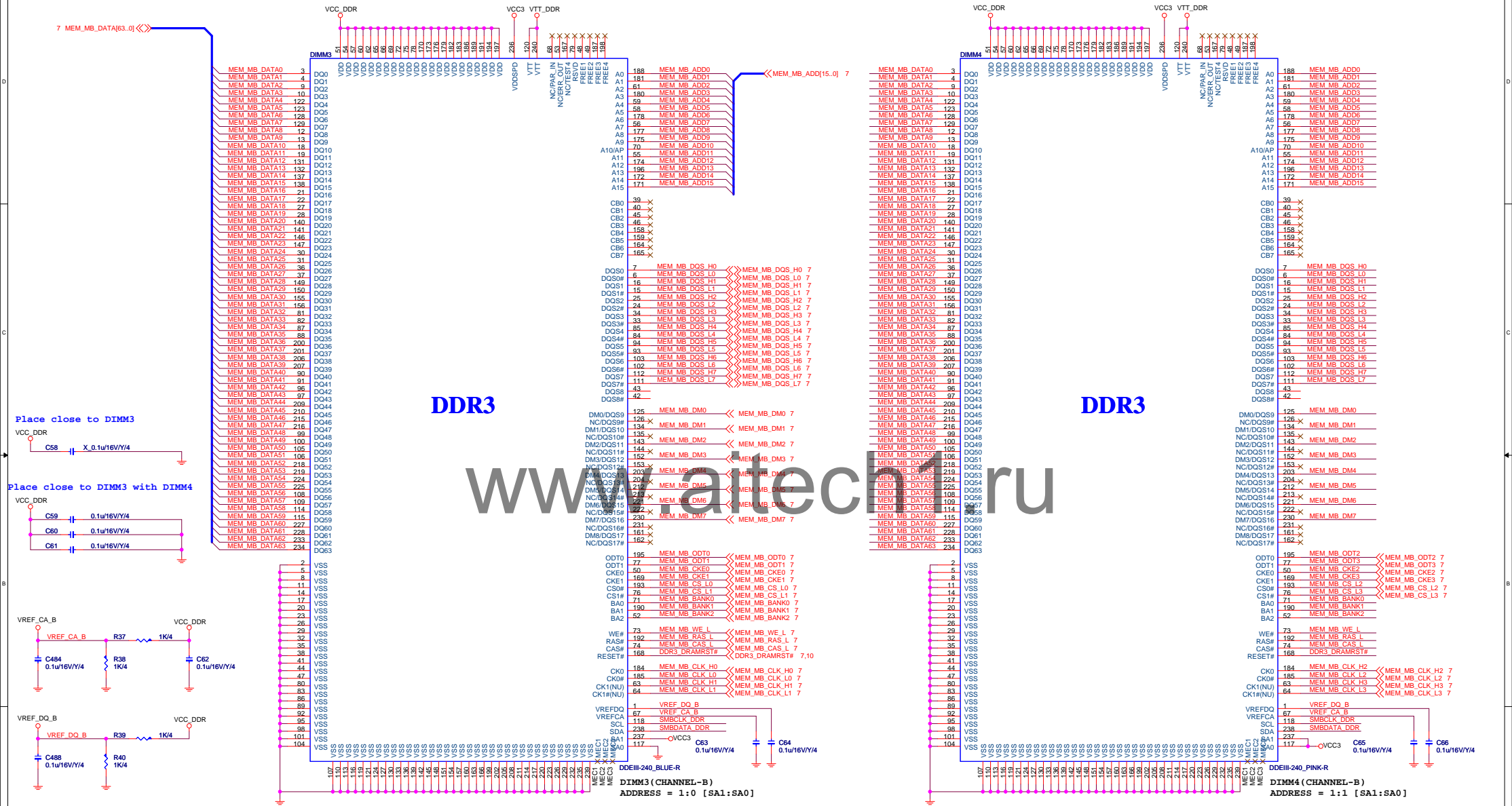
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DDR3 DIMM_B1

DDR3 DIMM_B2



Vref-DQ : Reference voltage for DQ0-DQ63, CB0-CB7 and PAR_IN. When in single ended mode used for DQS0-DQS7.

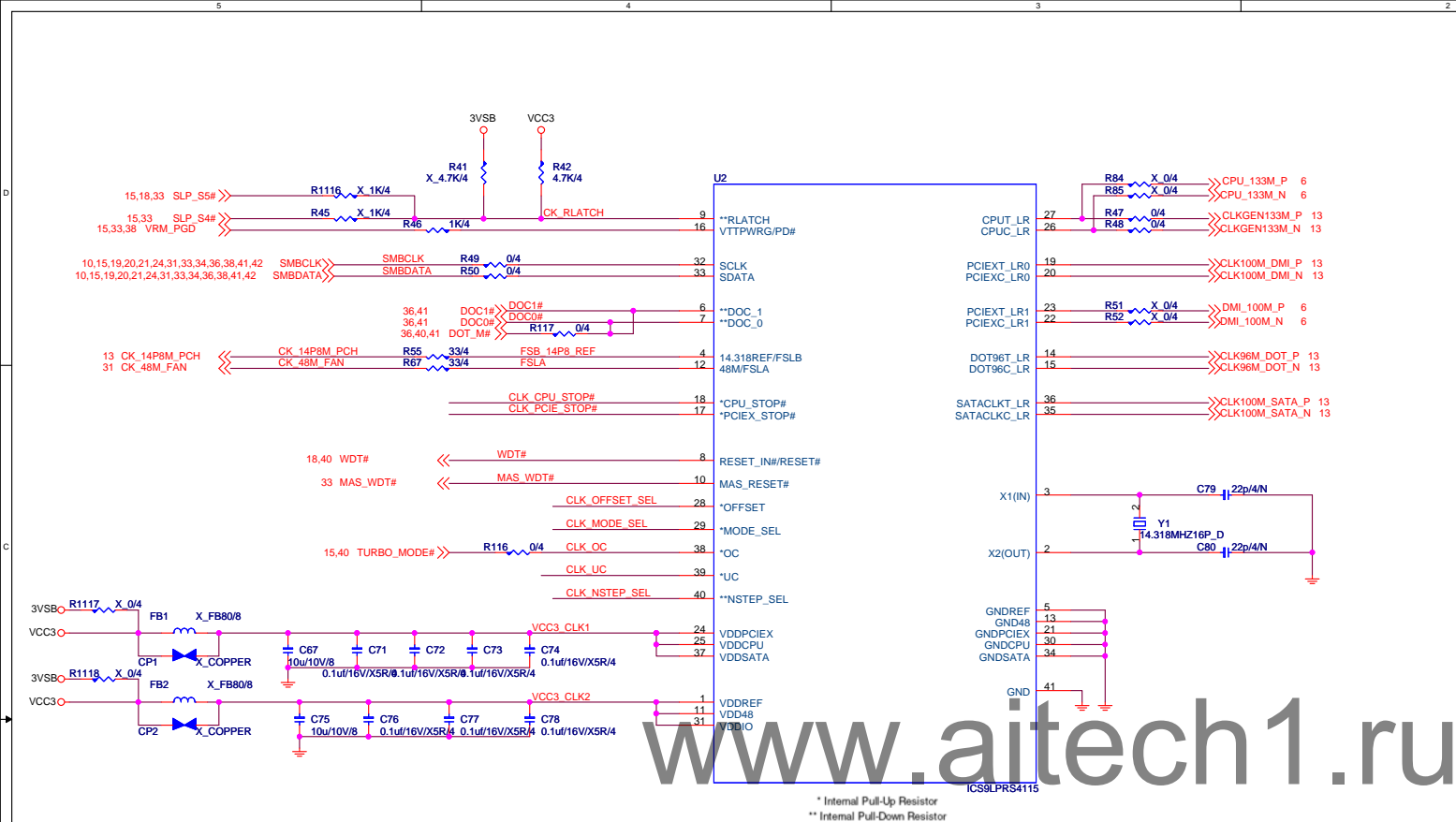
Vref-CA : Reference voltage for A0-A15, BA0-BA2, RAS#, CAS#, WE#, S0#, S01#, CKE0, CKE1, ODT0 and ODT1.

RESET#(Output) : A synchronously forces all registered output LOW when RESET# is LOW. This signal can be used during power up to ensure that CKE is LOW and DQs are High-Z.

—SMBCLK_DDR —SMBCLK_DDR 10
—SMBDATA_DDR —SMBDATA_DDR 10

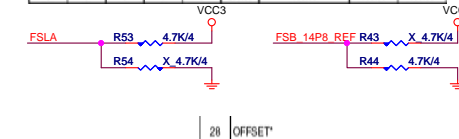


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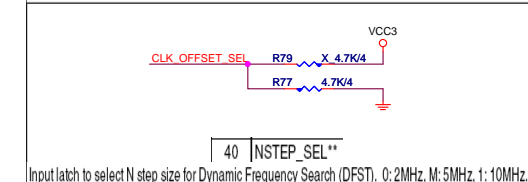


CLOCK GEN STRAPING

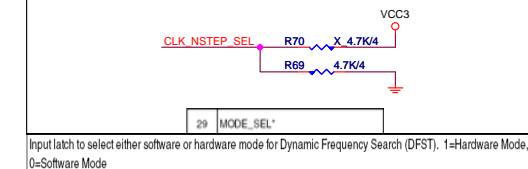
Functionality Table				CPU		PCIE	SATA
B44	B43	B42	B41	B40	MHz	MHz	MHz
F54	F53	F52	F51	F50	250.00	100.00	100.00
0	0	0	0	1	133.33	100.00	100.00
0	0	0	1	0	200.00	100.00	100.00



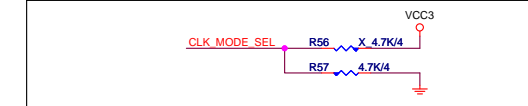
Input latch pin to set frequency offset from latch frequency for Dynamic Frequency Search (DFS). 1 = +200MHz offset at OC, -60MHz offset at UC. M = +150MHz offset at OC, -44MHz offset at UC. 0 = +100MHz offset at OC, -33MHz offset at UC.



Input latch to select N step size for Dynamic Frequency Search (DFS). 0: 2MHz, M: 5MHz, 1: 10MHz.



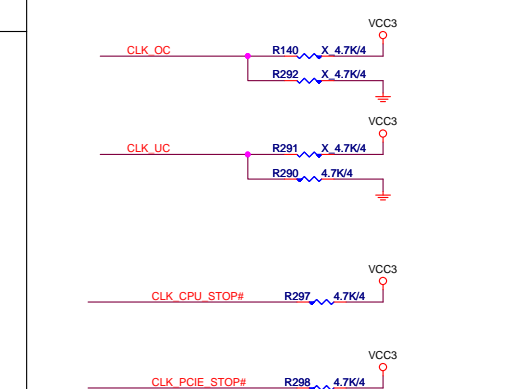
Input latch to select either software or hardware mode for Dynamic Frequency Search (DFS). 1=Hardware Mode, 0=Software Mode



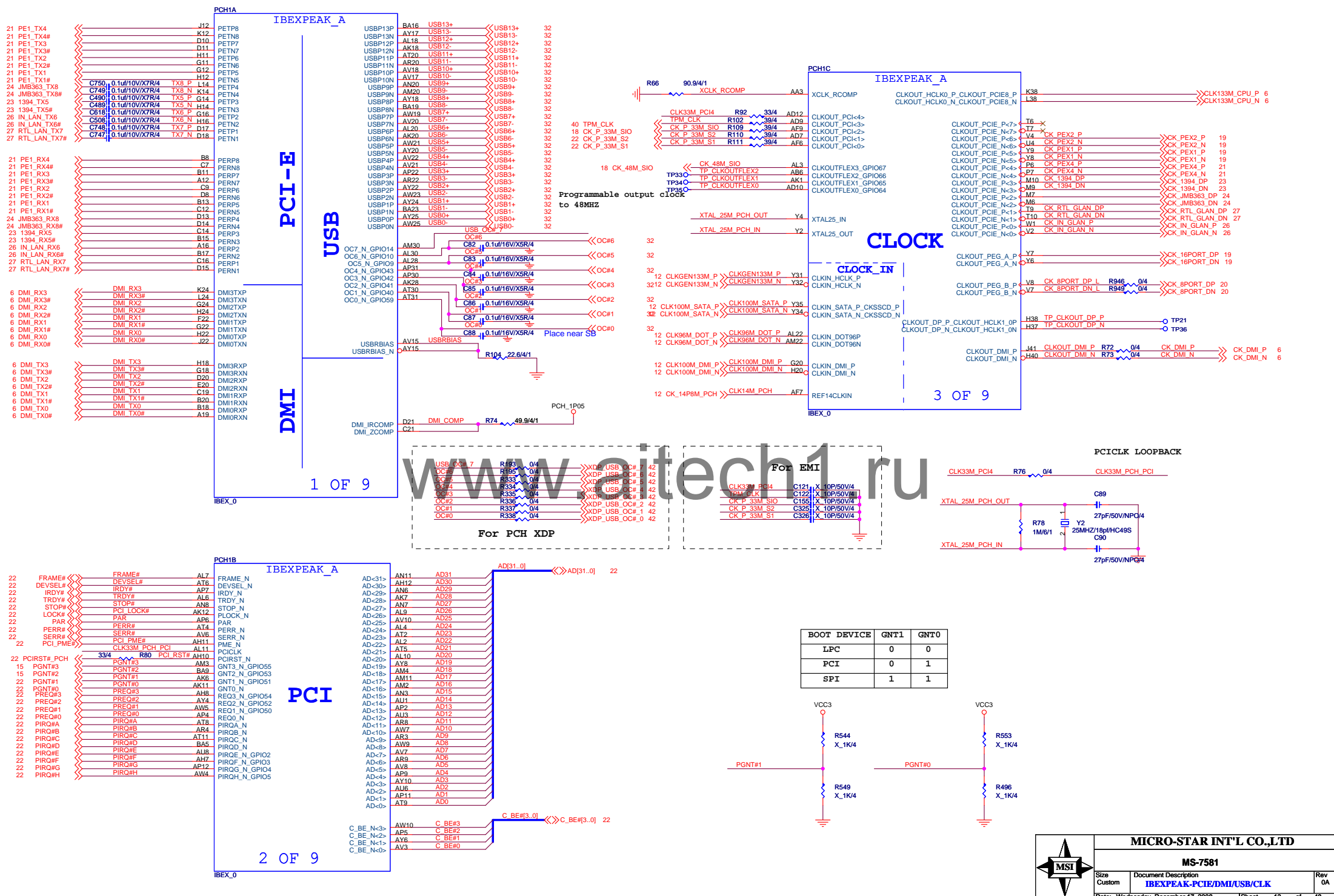
OC AND UC

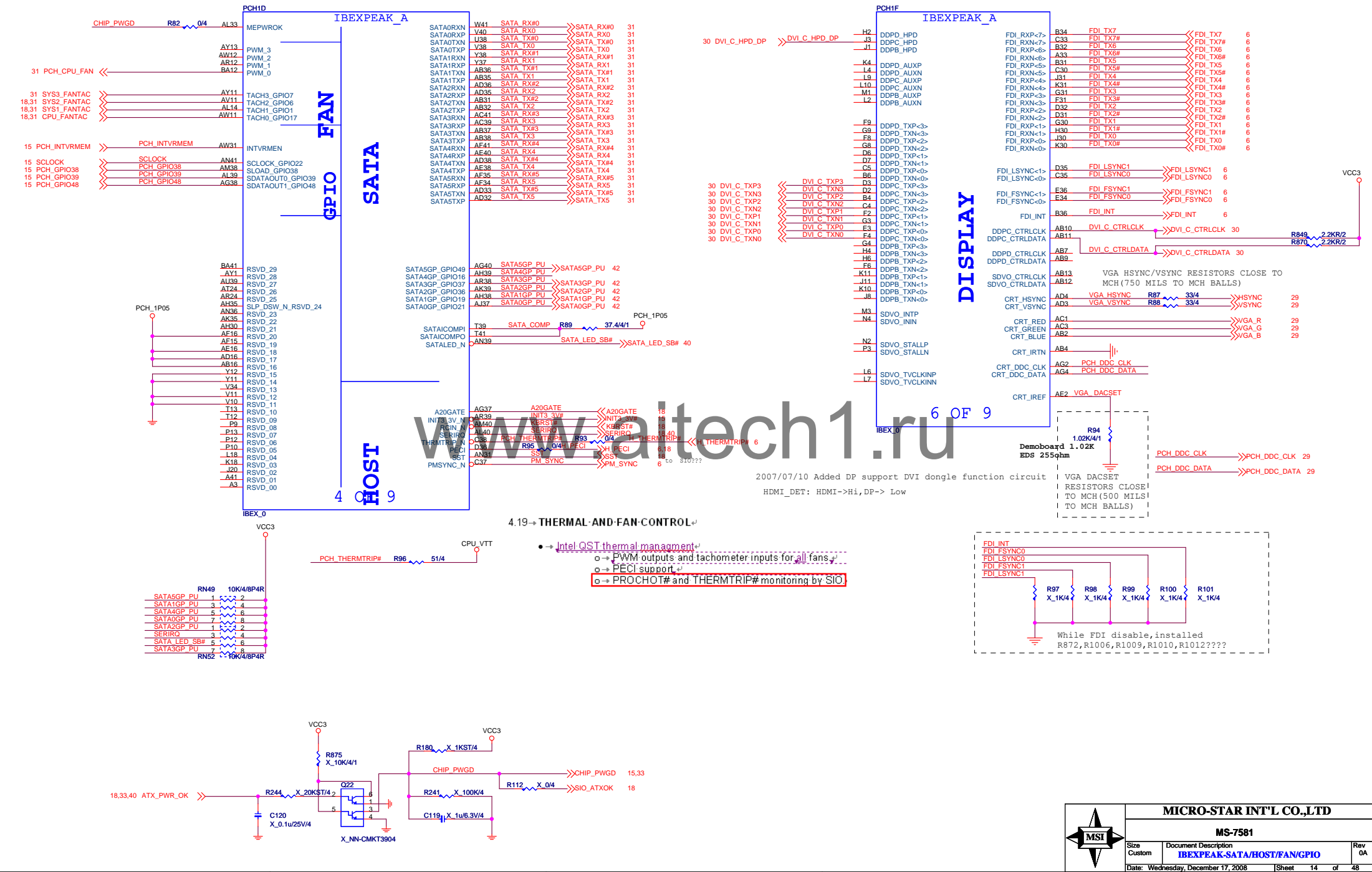
Input latch for Dynamic Frequency Search (DFS). Use in combination with UC pin. OC:UC=10 selects dynamic overlocking frequency search. OC:UC=01 selects dynamic underlocking frequency search. OC:UC=11 & 00 are invalid states and cannot be used.

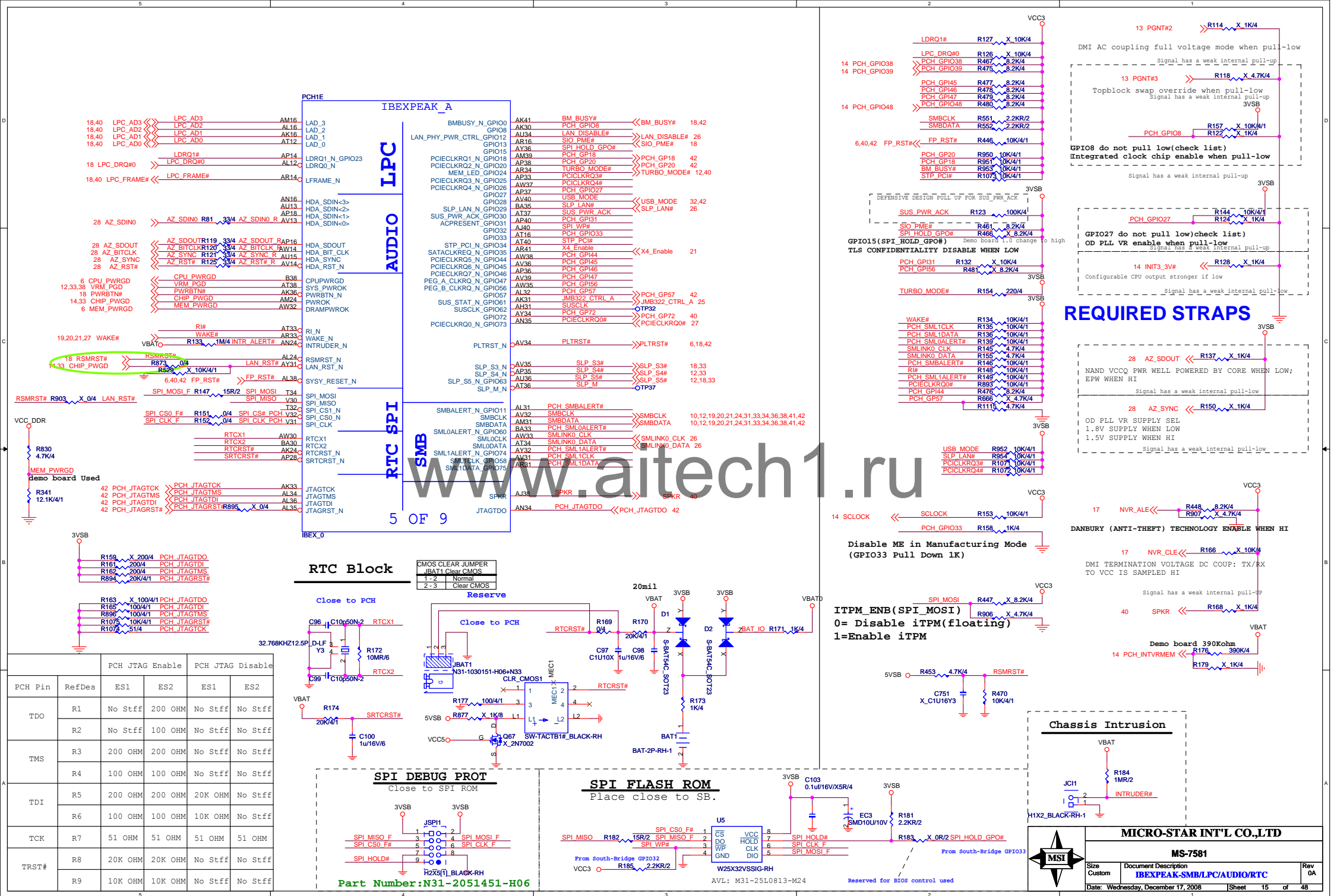
Input latch for Dynamic Frequency Search (DFS). Use in combination with OC pin. OC:UC=10 selects dynamic overlocking frequency search. OC:UC=01 selects dynamic underlocking frequency search. OC:UC=11 & 00 are invalid states and cannot be used.

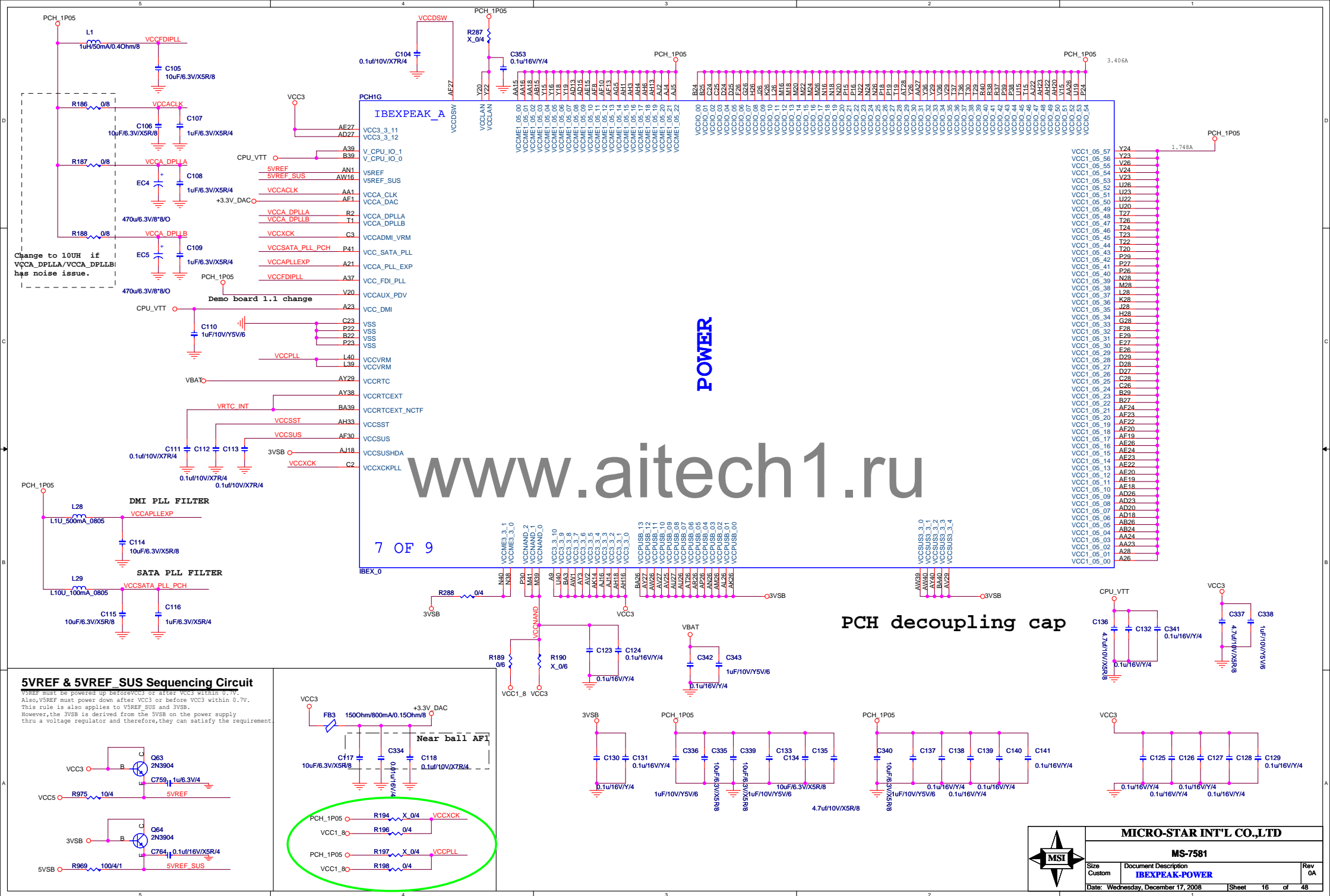


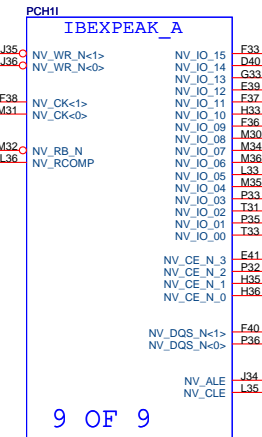
MICRO-STAR INT'L CO.,LTD		
MS-7581		
Size	Document Description	Rev
Custom	Clock Gen ICS9LPRS4100	0A
Date: Wednesday, December 17, 2008	Sheet 12 of 48	





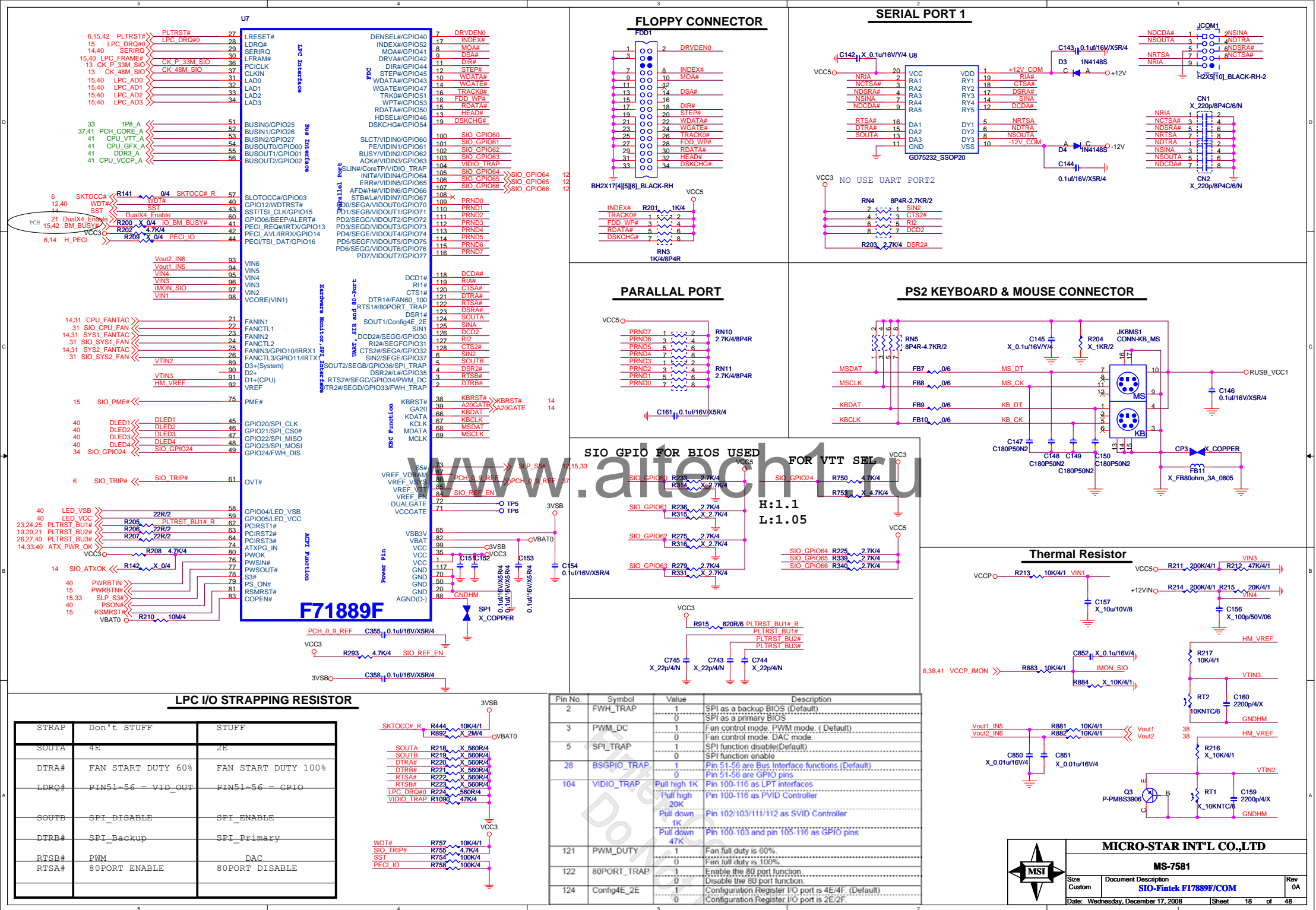




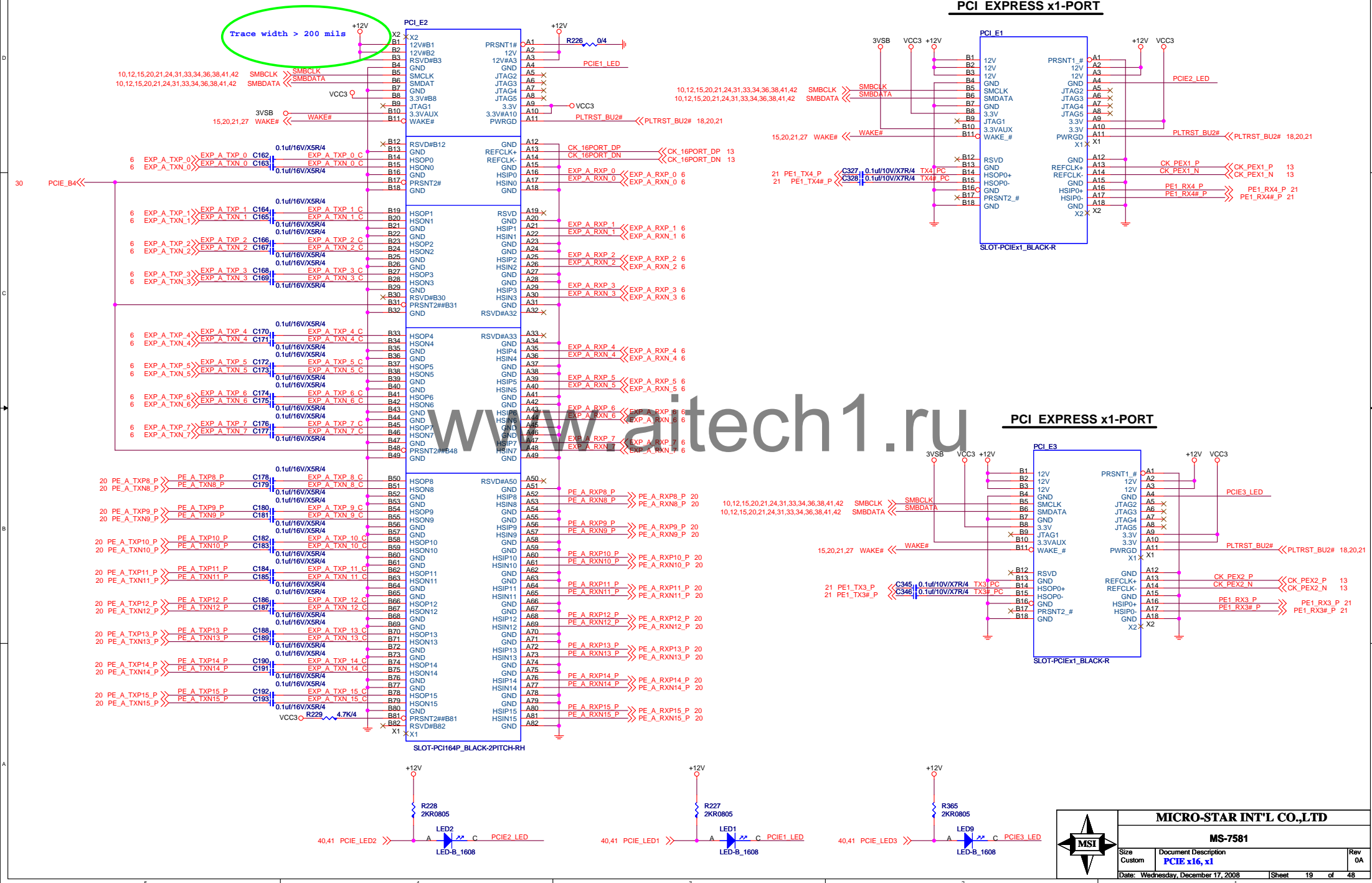


9 OF 9

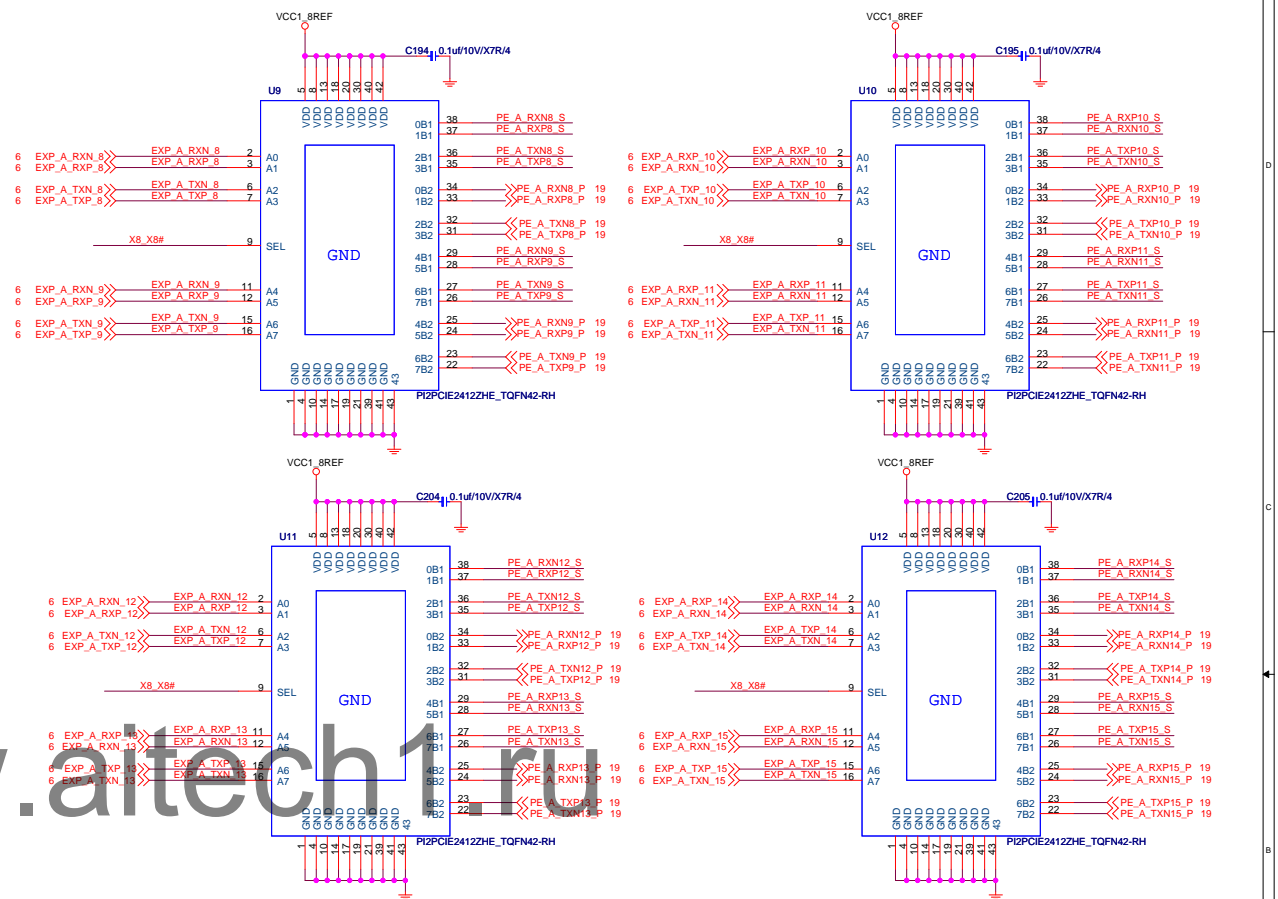
NV_ALE	J34	NVR_ALE	NVR_ALE	15
NV_CLE	L35	NVR_CLE	NVR_CLE	15



PCI_Express X16 Slot



(Share with PCI_E x16 Slots)



	Low	B1	Low	X8 / X8
	B1	B2	B1	X16

VCC3

VCC1_8REF

R234
4.7K/4

R235
4.7K/4

XB_X8#

XB_X8

R237 0/4

Q4 N-MMBT3904_NL_SOT23

DualX8_Enable

DualX8_Enable

C214 0.1uF/10V/XR

C215 0.1uF/10V/XR

C216 0.1uF/10V/XR

C217 0.1uF/10V/XR

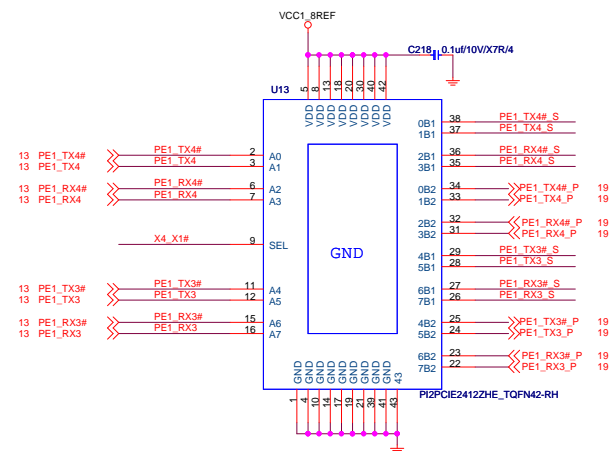
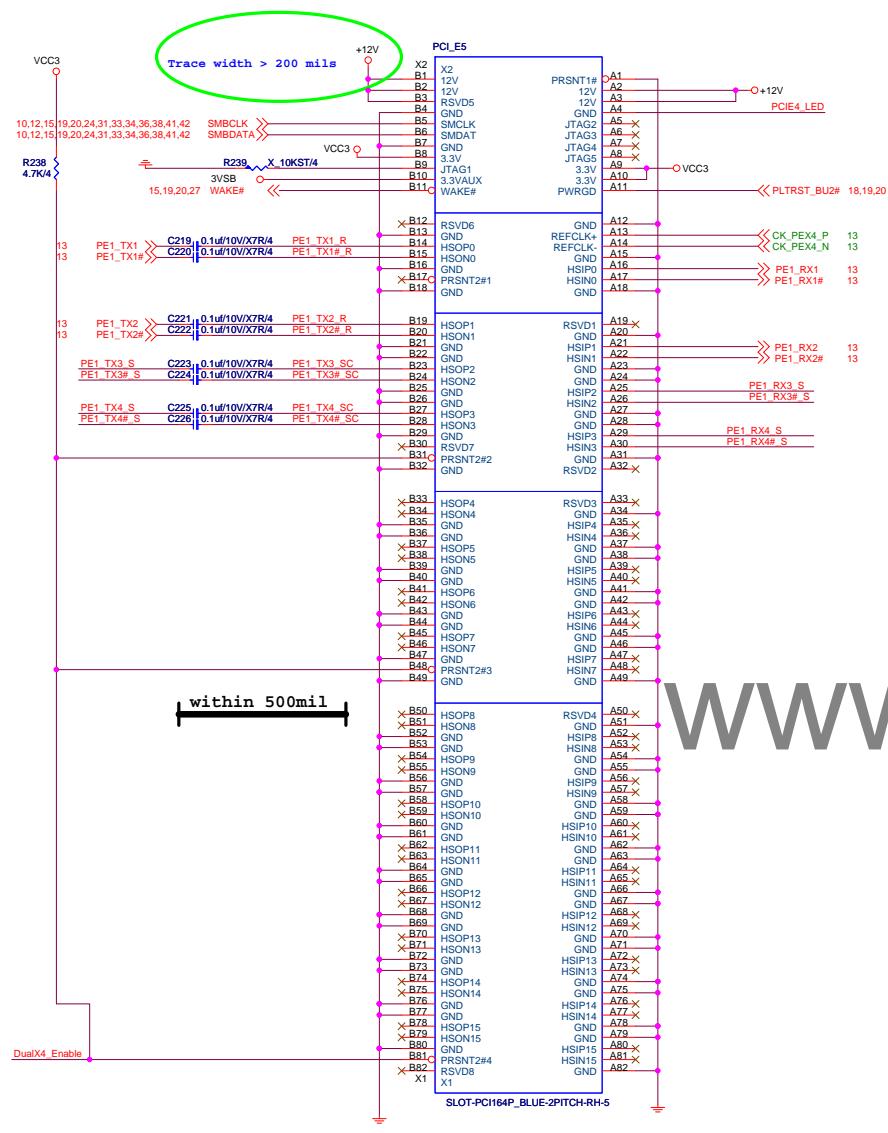


MS-7581

Size Custom	Document Description PCIEx8/Pericom switch	Rev 0A
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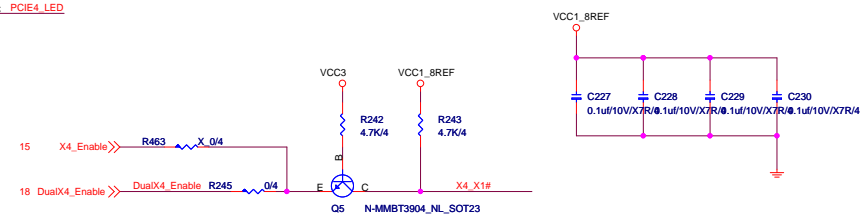
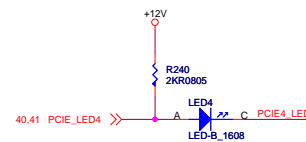
Date: Wednesday, December 17, 2008	Sheet 20 of 48
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PCI_Express X4 Slot
(Share with PCI_E x1 Slots)



Digital Switch	
SEL pin	SLI function

SEL (DualX8 Enable)	Output	X4 SW	PCI-E Slot 1/2
Low	B1	Low	X4
Hi	B2	Hi	X1 / X1



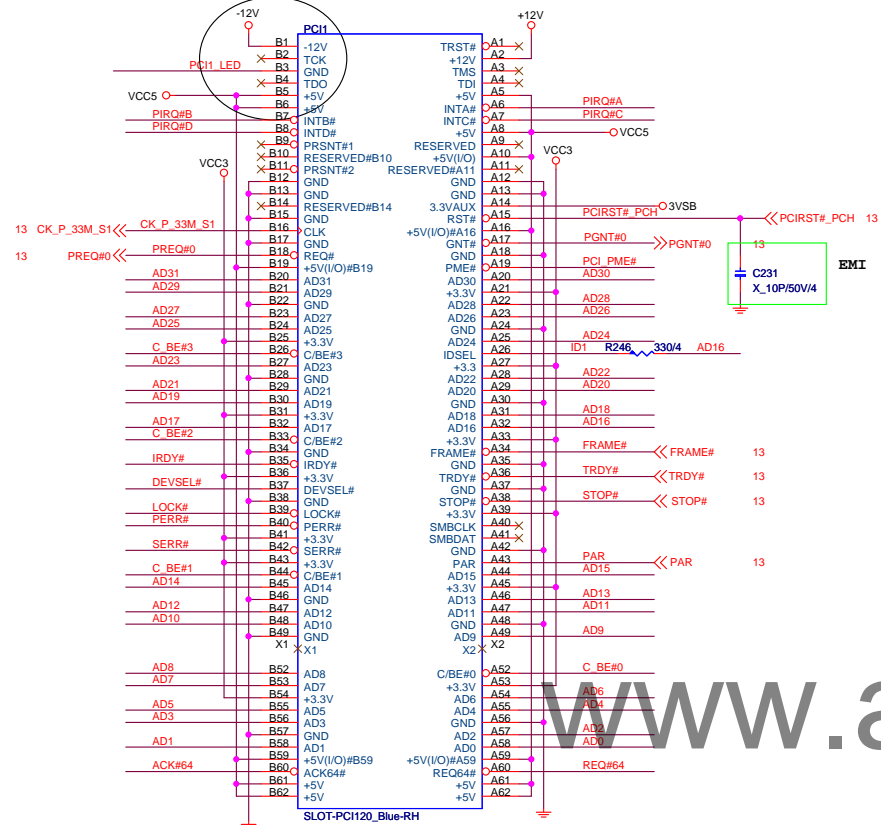
MICRO-STAR INT'L CO.,LTD

MS-7581

Size Custom	Document Description PCIEx8/Pericom switch	Rev 0A
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Date: Wednesday, December 17, 2008 Sheet 21 of 48

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



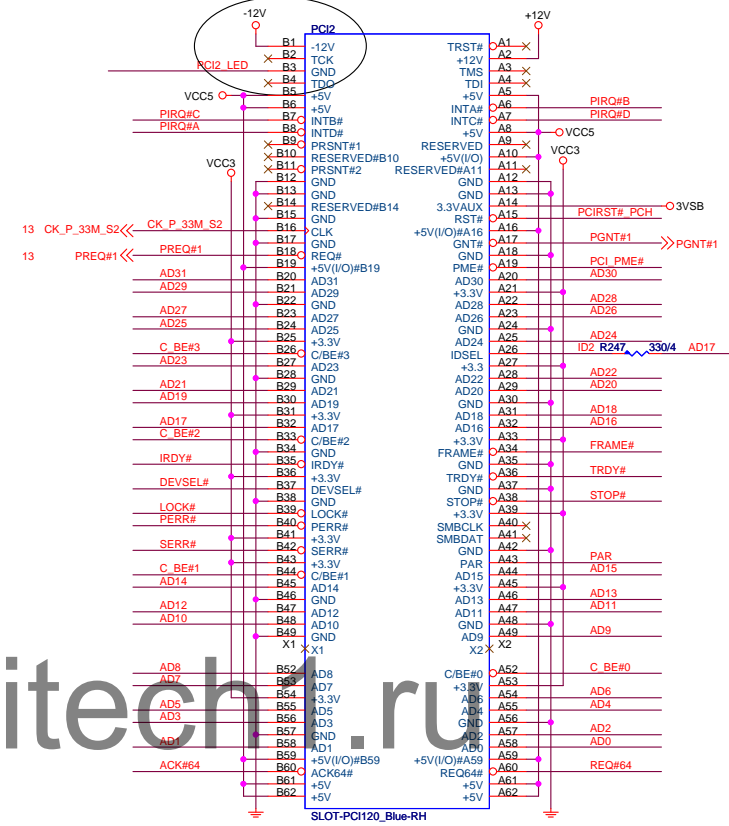
```

IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

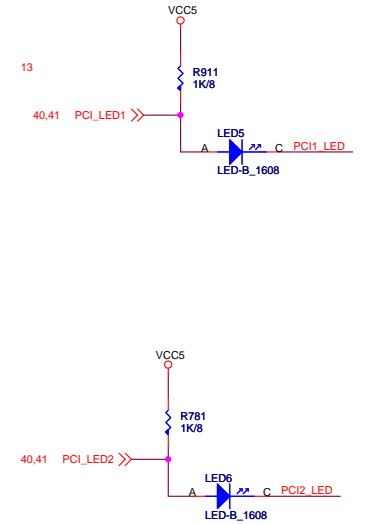
```

13 AD[31..0] << AD[31..0]

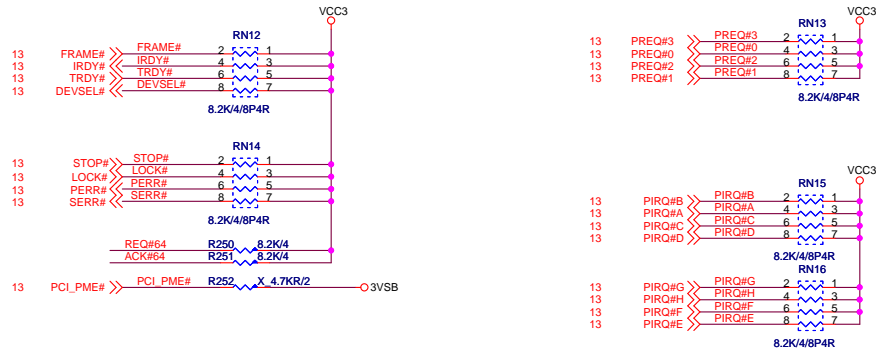
13 C_BE#[3..0] << C_BE#[3..0]



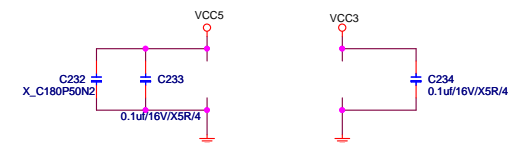
```
IDSEL = AD17
MASTER = PREQ#1
PIRQ#B
```



PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS

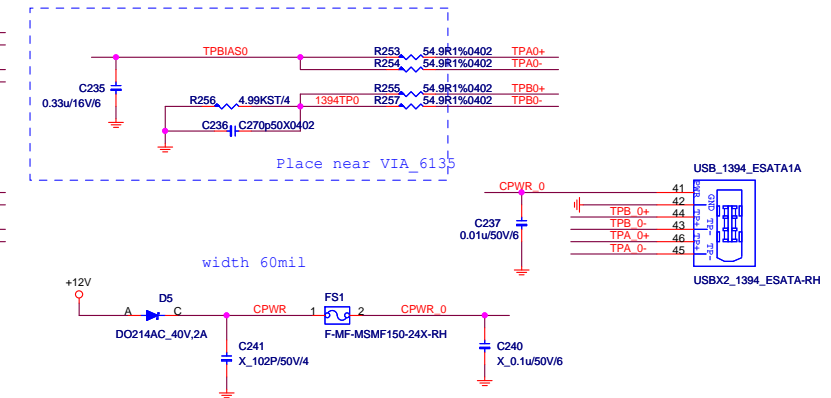
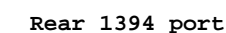
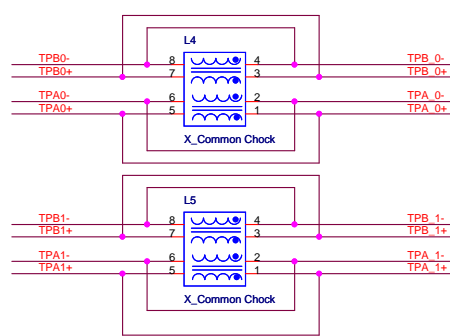
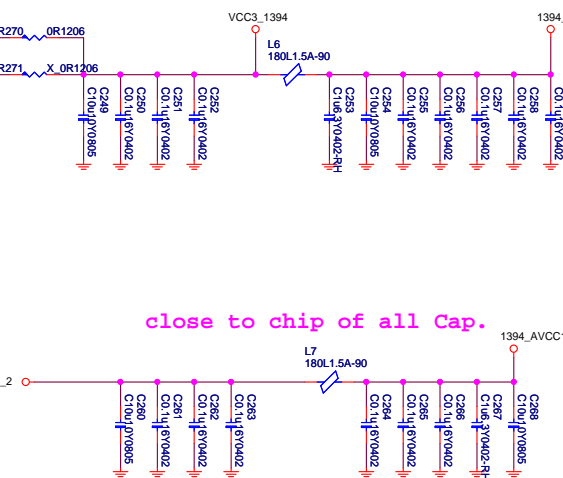
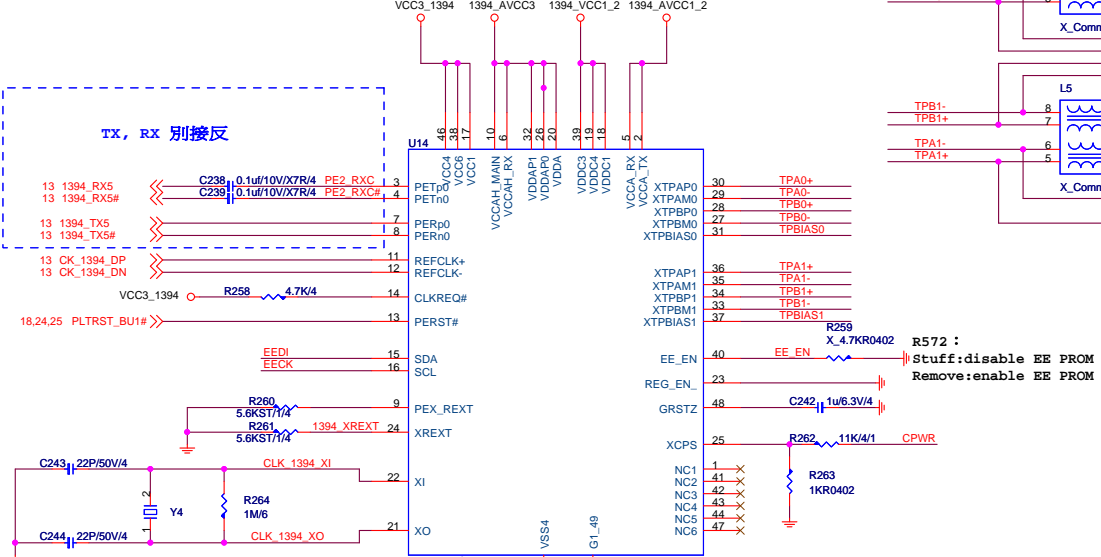


MICRO-STAR INT'L CO.,LTD

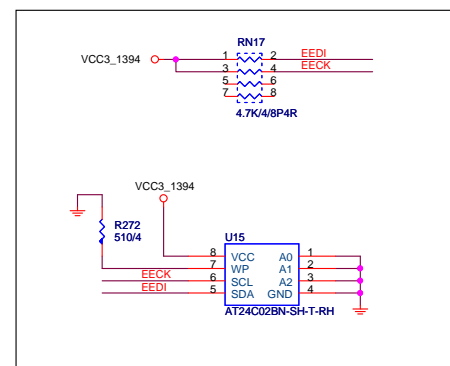
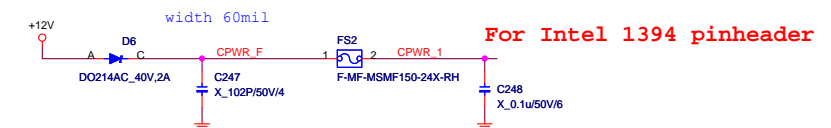
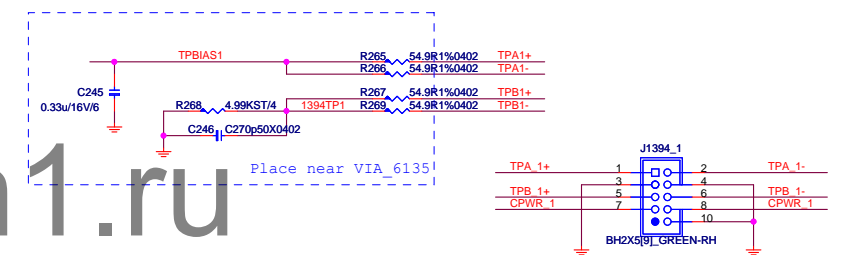
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Size Custom	Document Description PCI Slot 1 & 2	Rev 0A
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1394 CONTROLLER



Front 1394 pin header

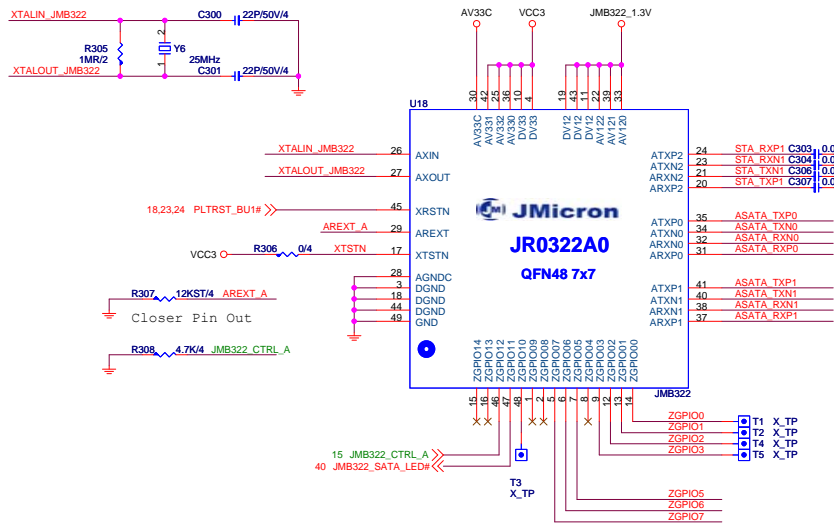


MICRO-STAR INT'L CO.,LTD

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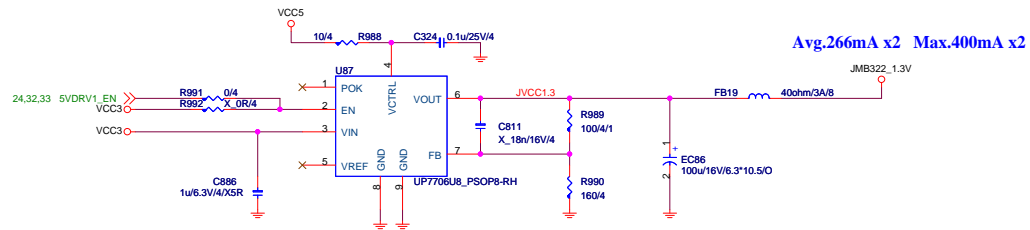
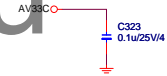
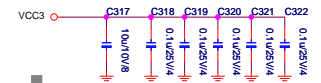
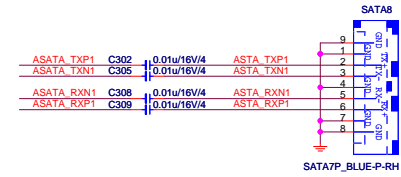
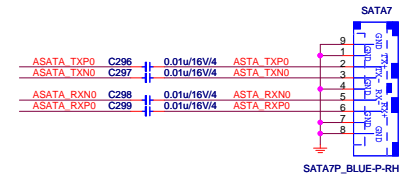
Size Custom	Document Description 1394 Controller - VT6315N-CD	Rev 0A
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JMB322 - H/W RAID CONTROLLER A



```
GPIO5
H : SETTING
L : NORMAL

GPIO7 GPIO6
0      0      RAID0
0      1      RAID1
1      0      JBOD
1      1      CLEAR RAID
```



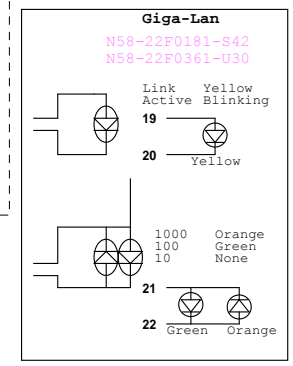
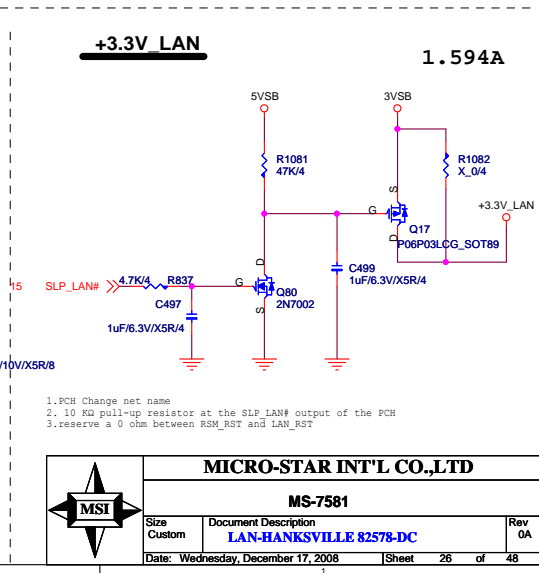
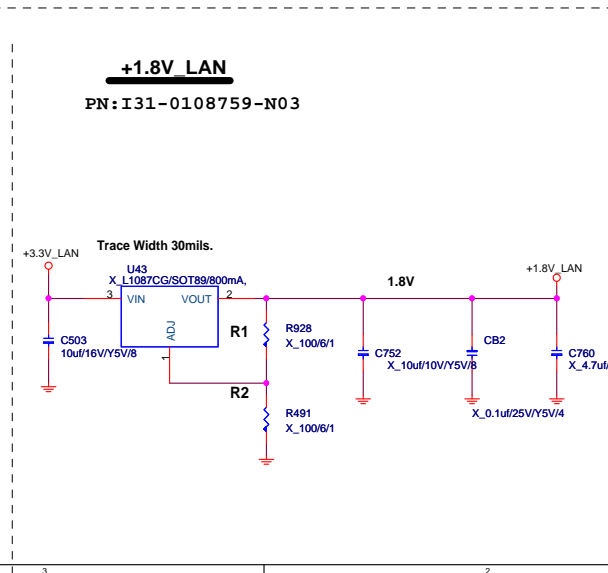
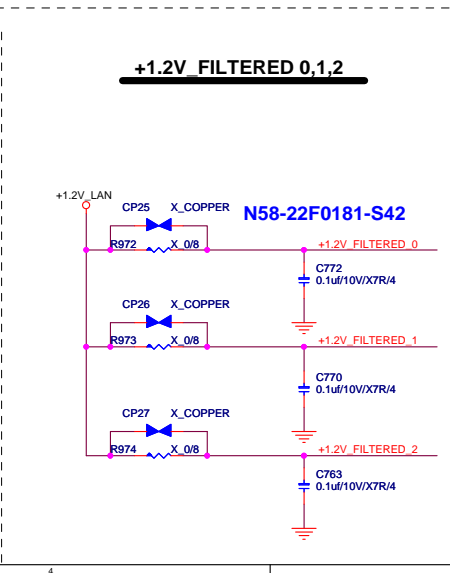
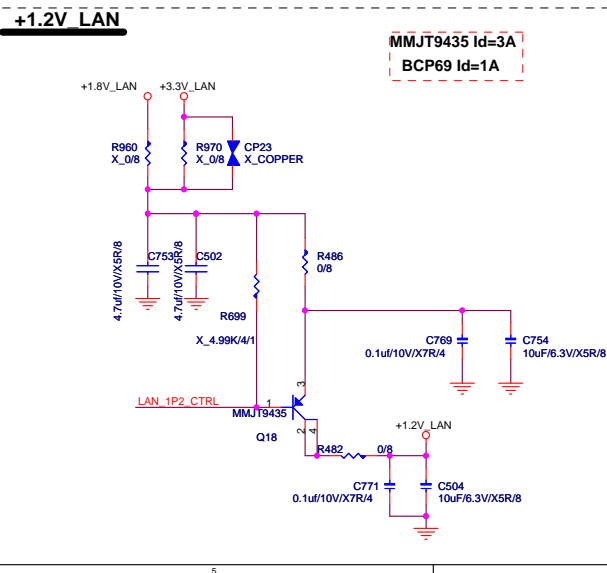
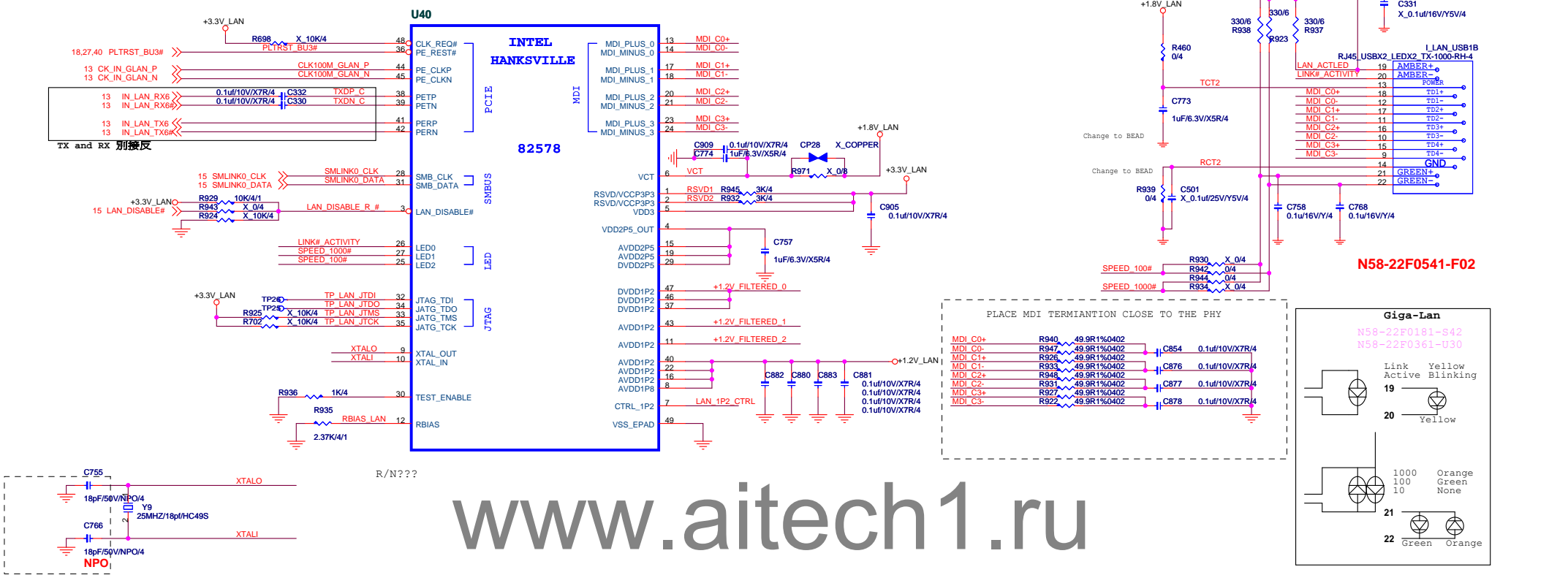
MICRO-STAR INT'L CO.,LTD

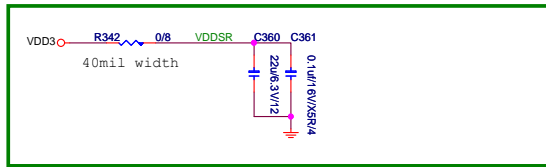
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Size Custom	Document Description JMB362 PCIE to PATA/SATA
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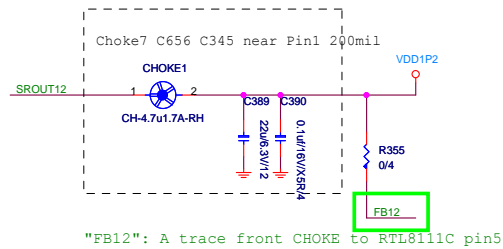
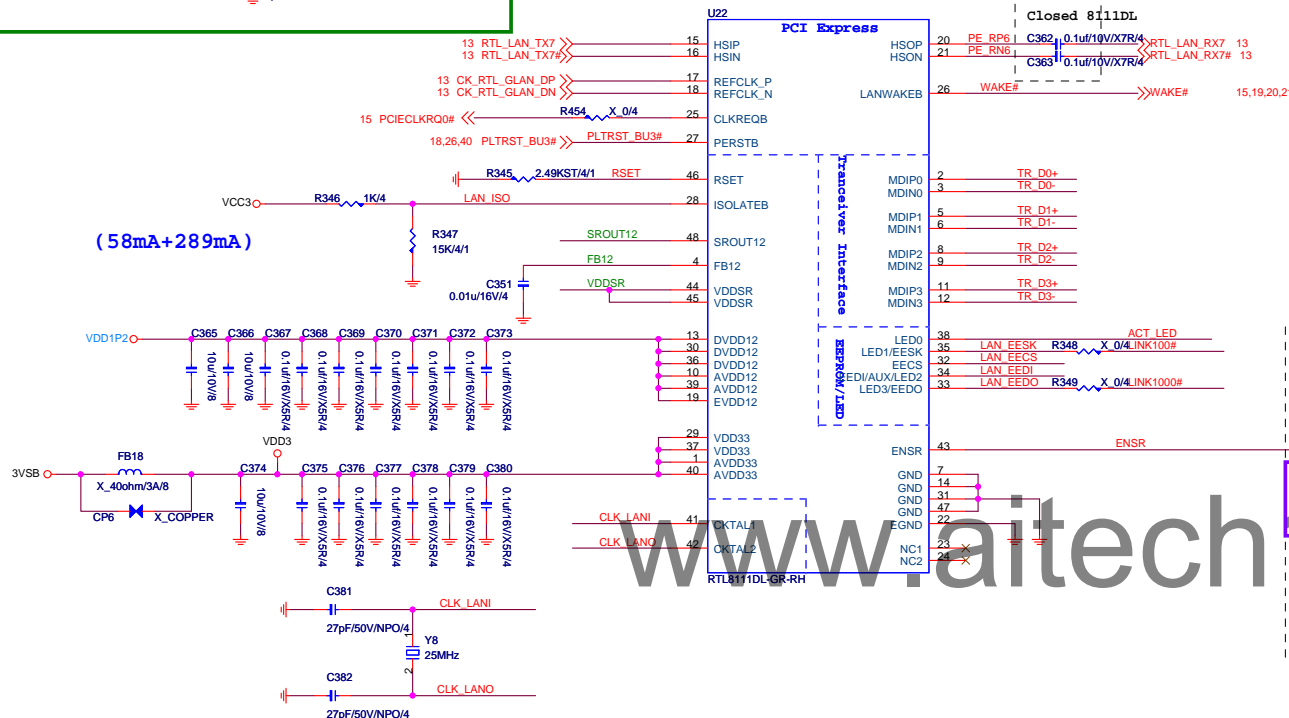
Date: Wednesday, December 17, 2008 Sheet 25 of 48

$$V_o = V_{ref}(1+R_2/R_1) + I_{adj} \times R_2$$

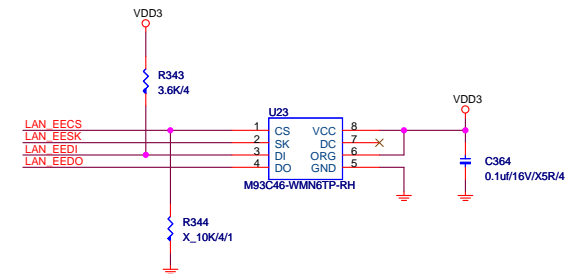
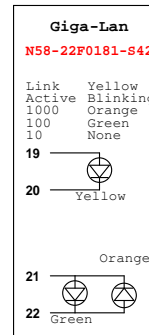
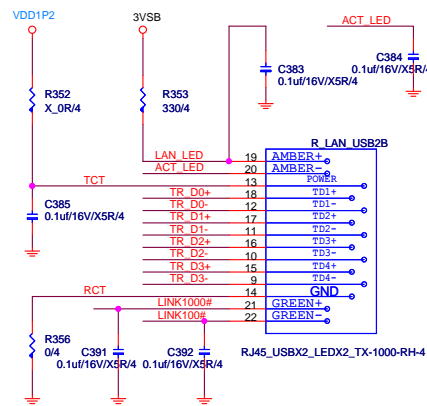




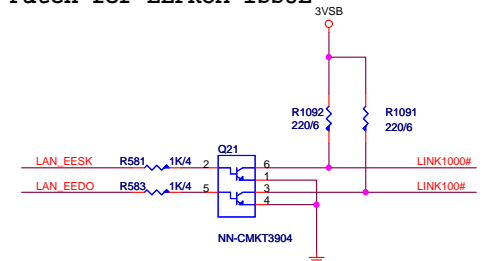
(58mA+289mA)



"FB12": A trace front CHOKE to RTL8111C pin5

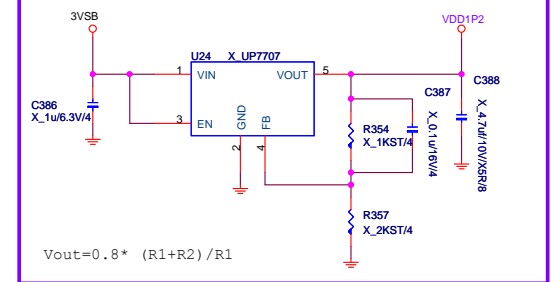


Patch for EEPROM ISSUE

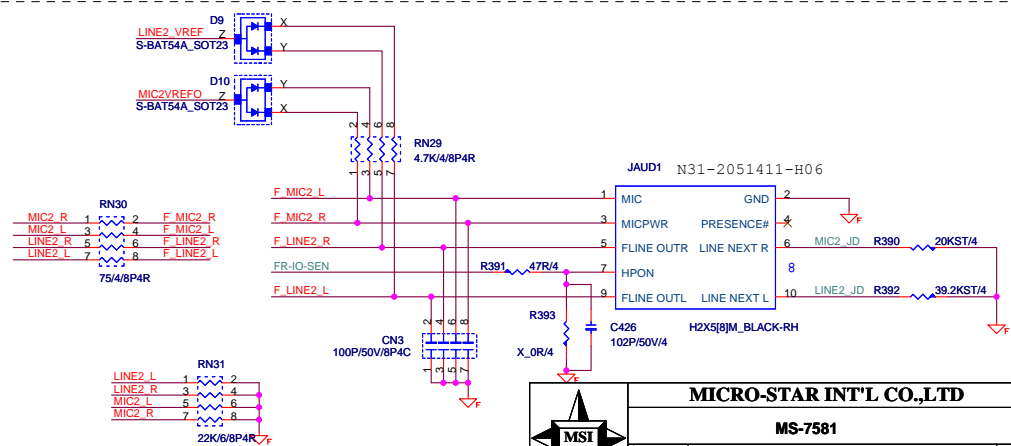
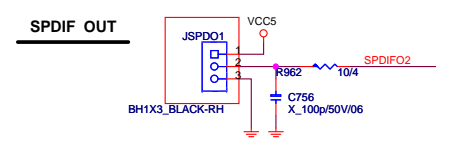
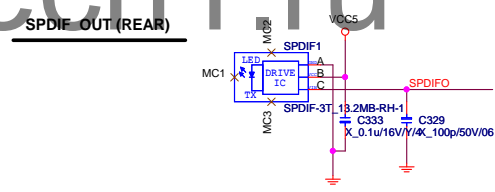
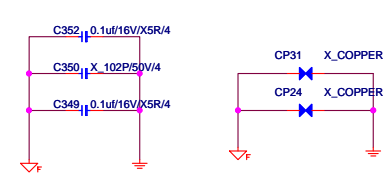
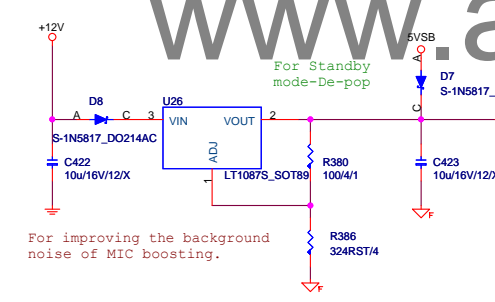
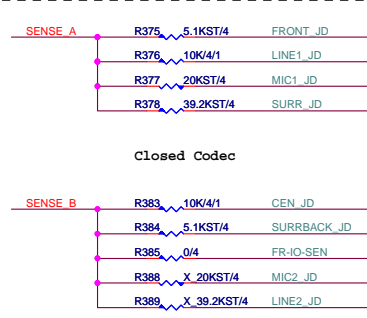
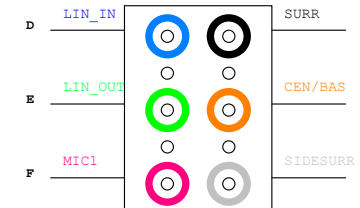
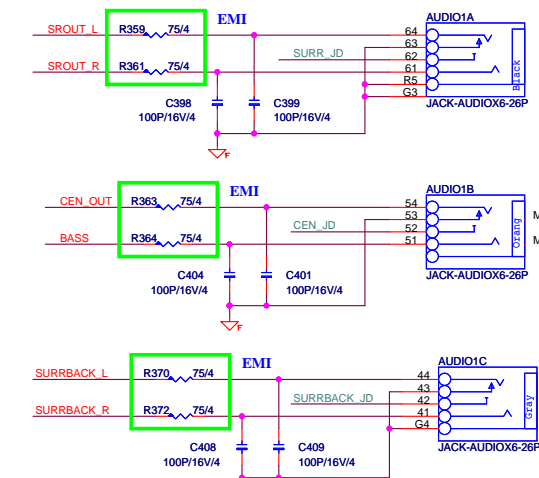
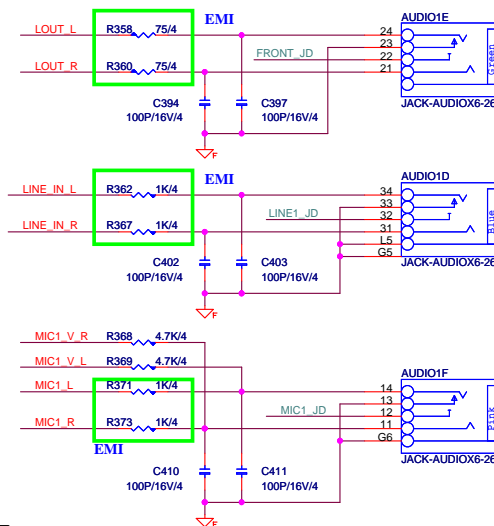
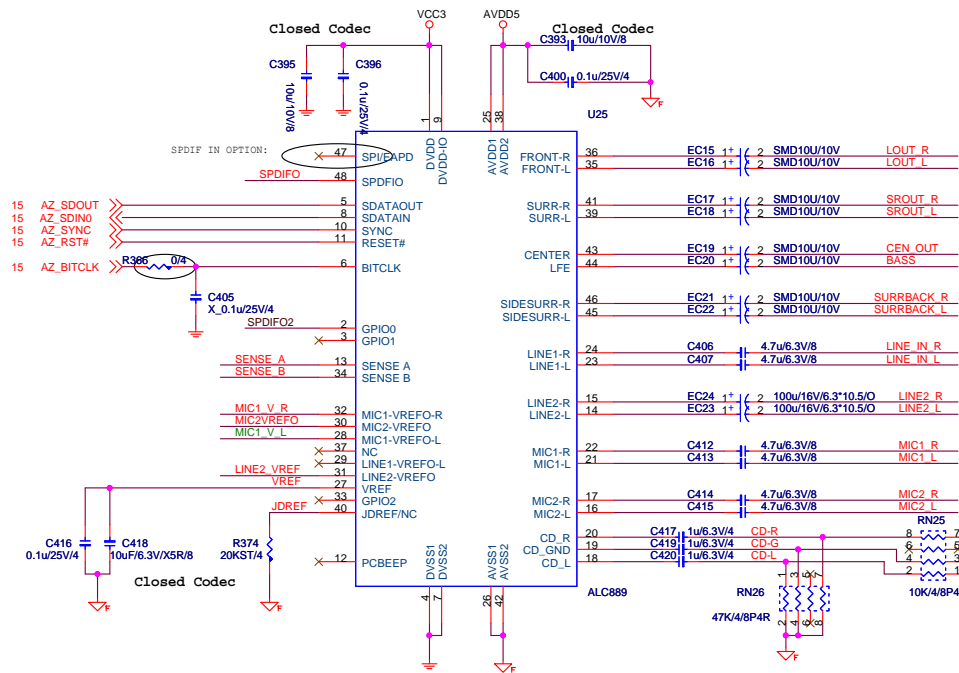


ENSR=1,
Enable switching regulator
ENSR=0,
Disable switching regulator

8111DL switching regulator disabled

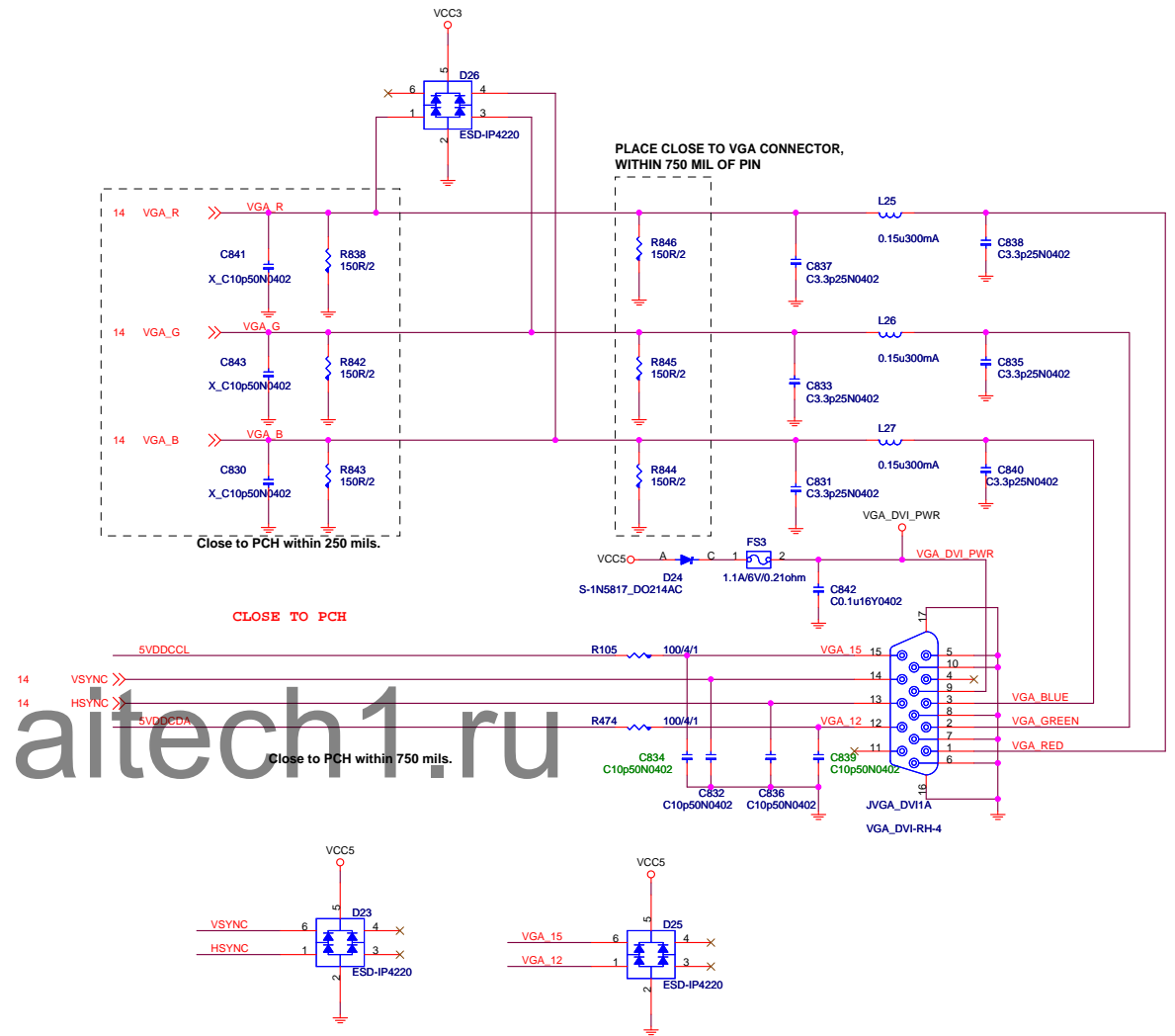
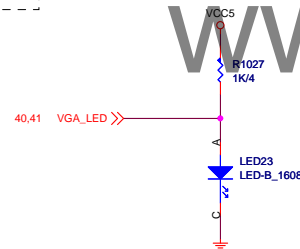
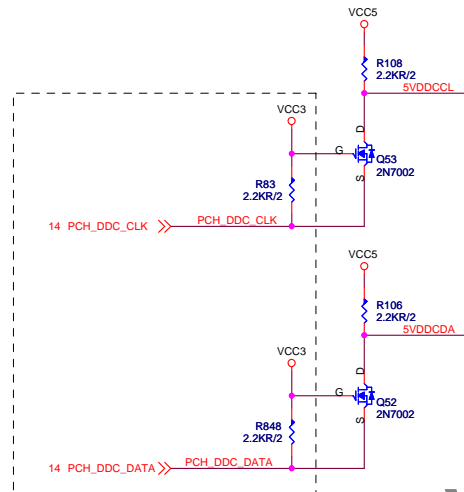


Vout=0.8 * (R1+R2) / R1



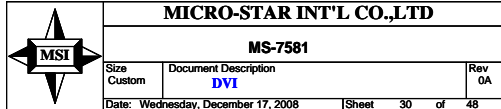
MICRO-STAR INT'L CO.,LTD			
MS-7581			
Size	Document Description	Rev	
Custom	Audio Codec ALC889	0A	
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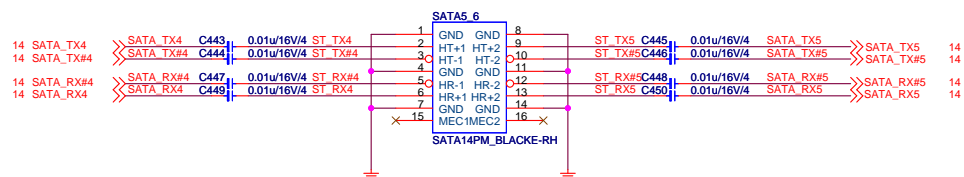
Video Connector



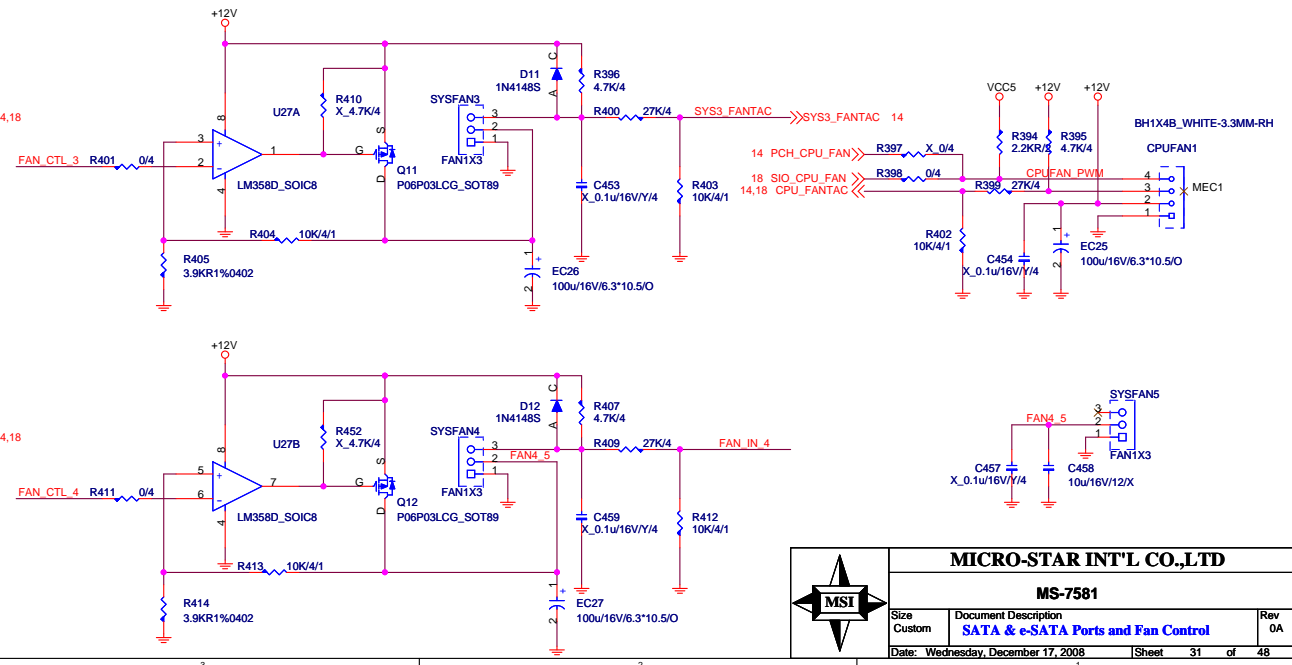
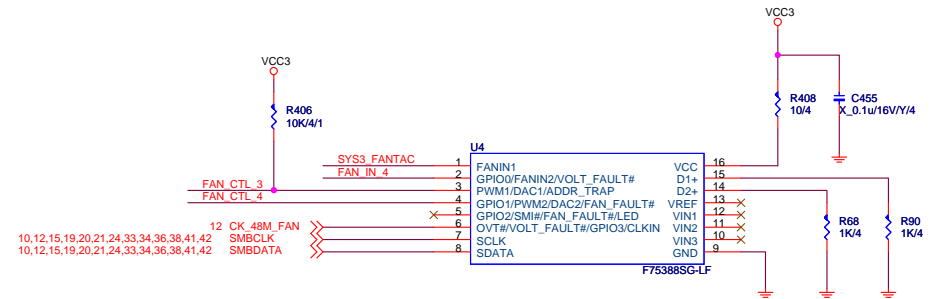
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(Share PCI_E x4 form PCI_E x16 Slots)



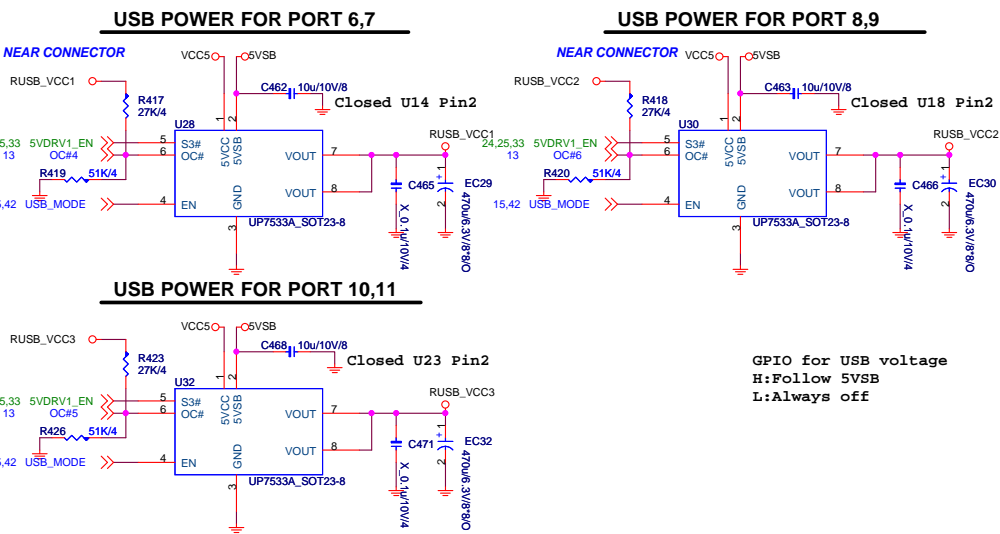


FAN initial Speed setting(PIN3)

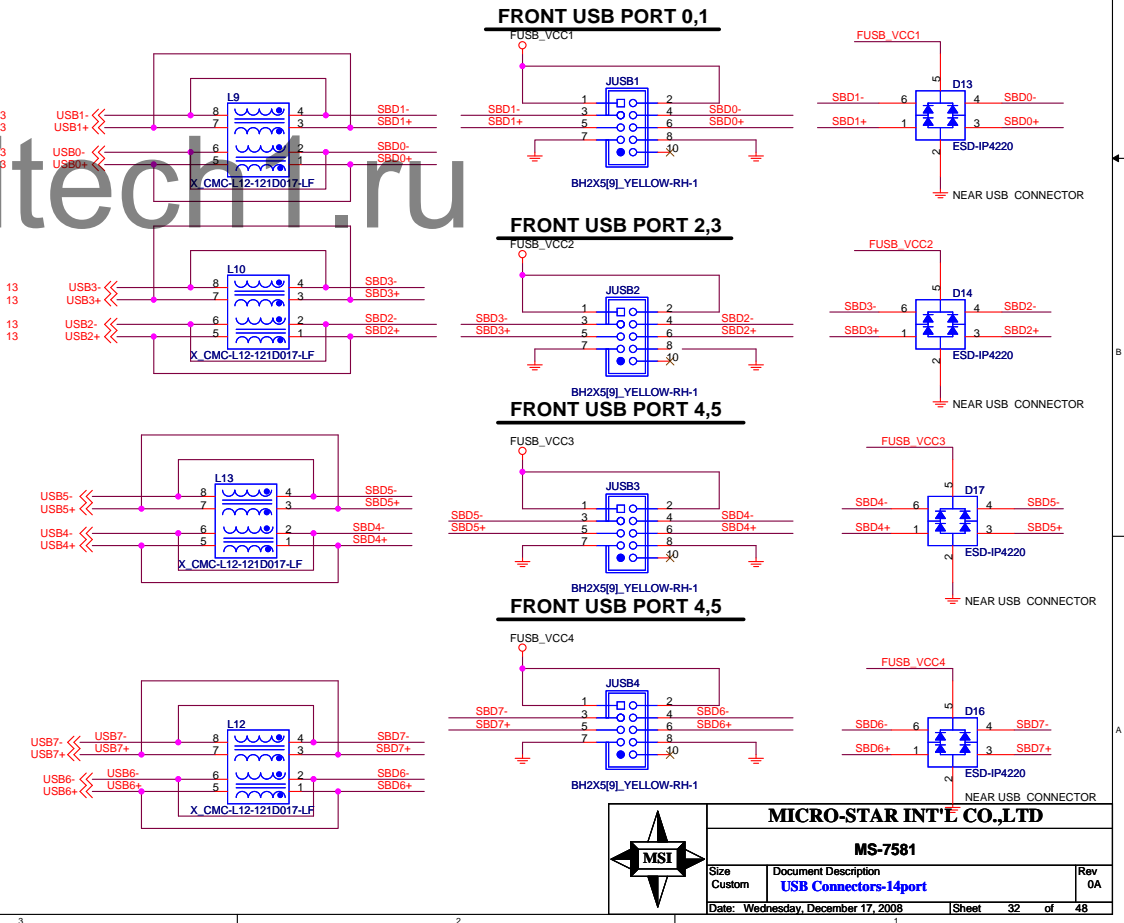
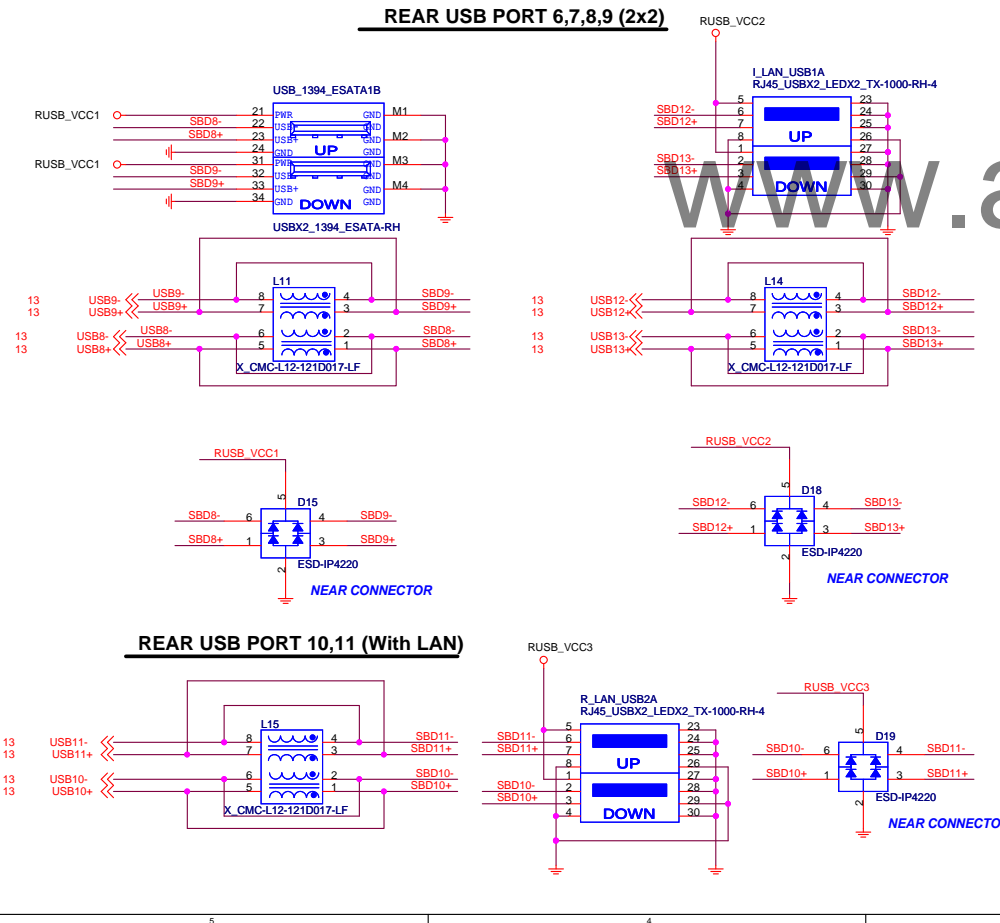
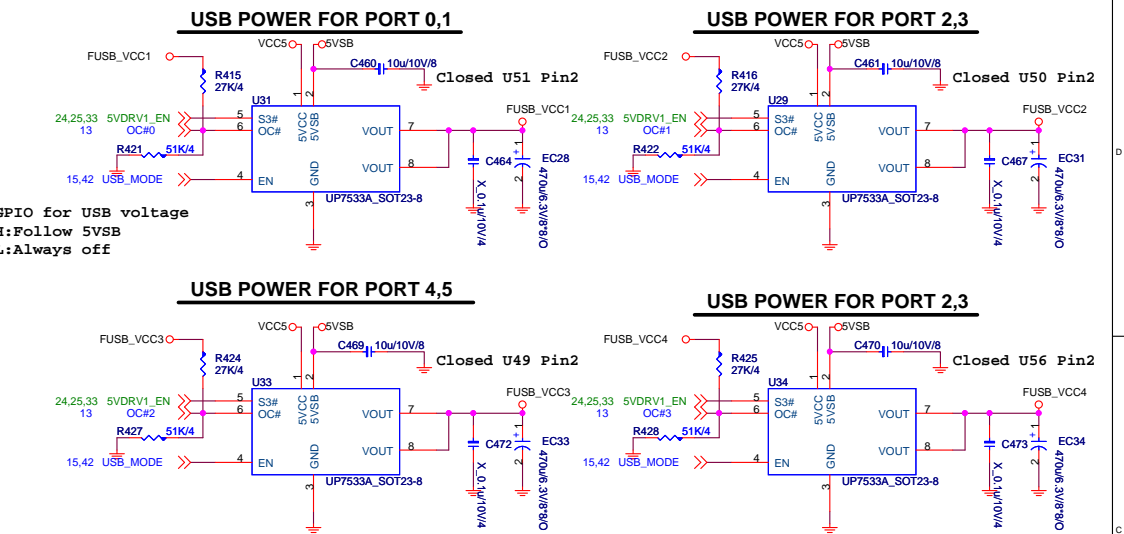


Size Custom	Document Description SATA & e-SATA Ports and Fan Control	Rev 0A
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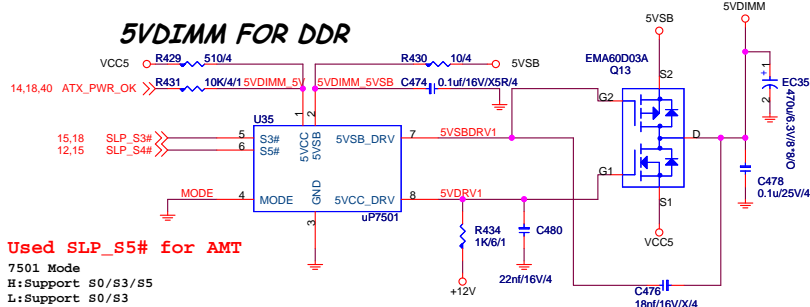
Rear USB Connector



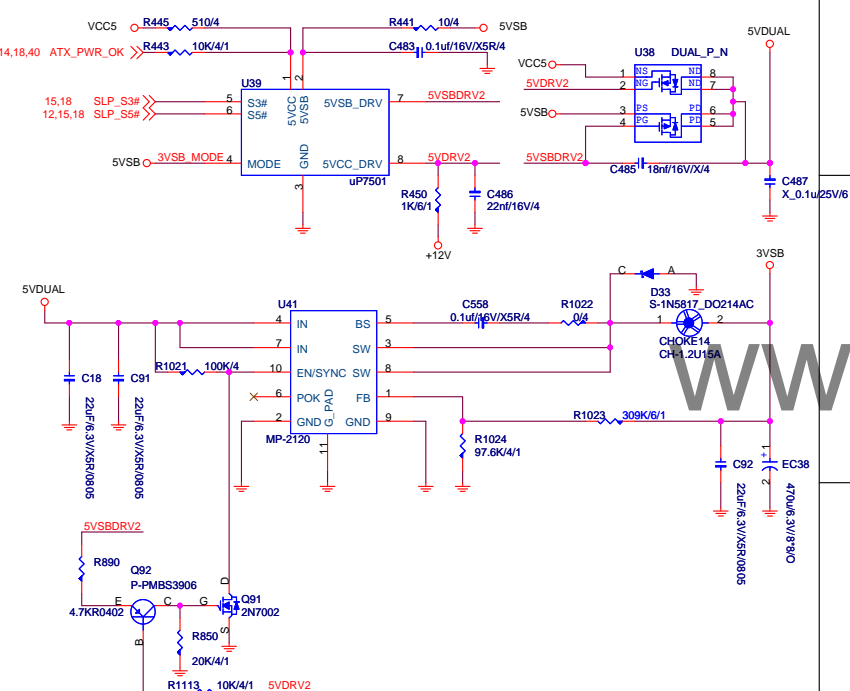
Front USB Connector



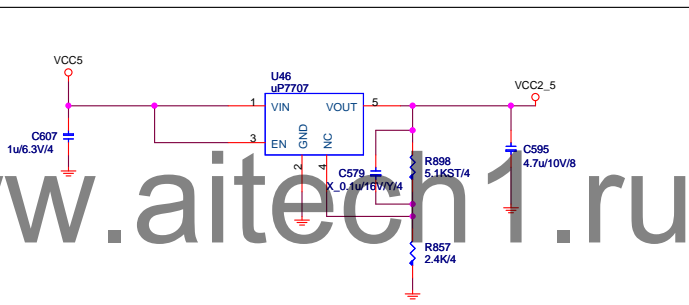
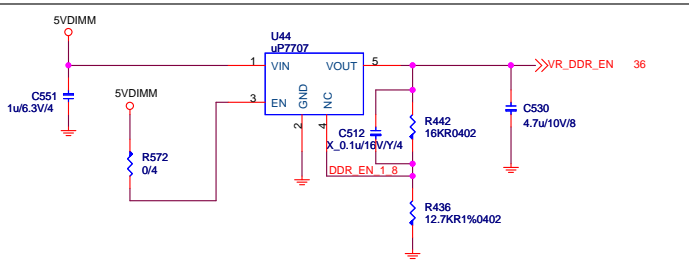
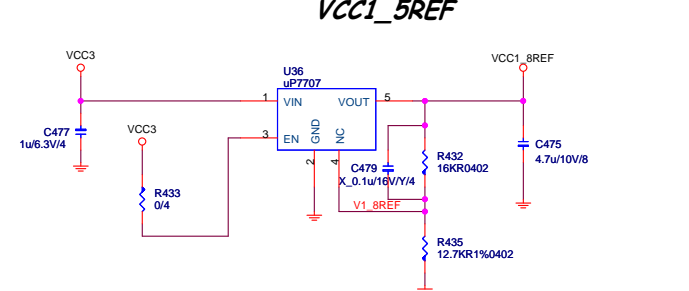
5VDIMM FOR DDR



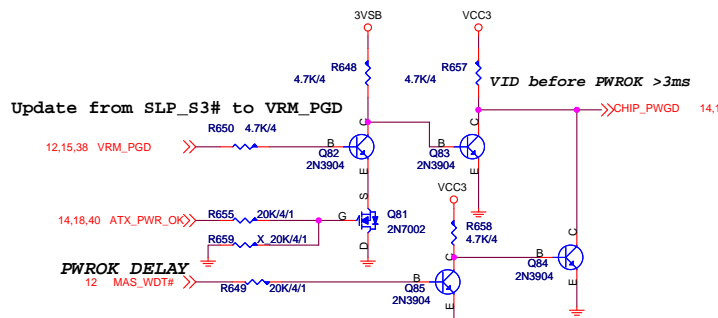
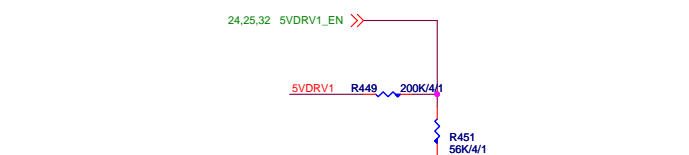
3VSB

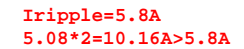


VCC1_5REF



USB MODE





VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOLTAGE
0	1	0	1	0	0	1	0	1.10000
0	1	0	1	1	0	1	0	1.05000

UPI VOLTAGE CONSOLE

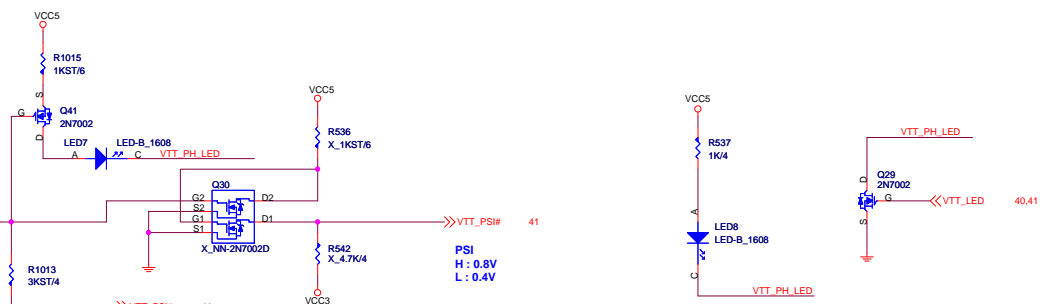
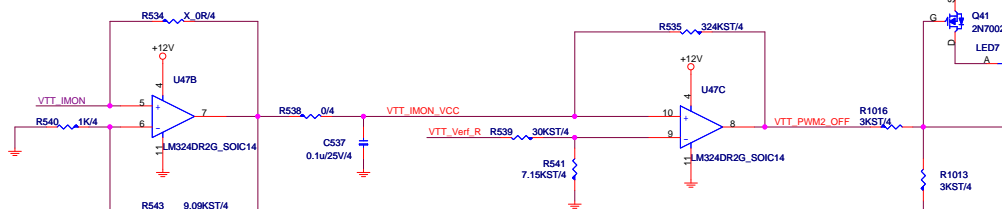
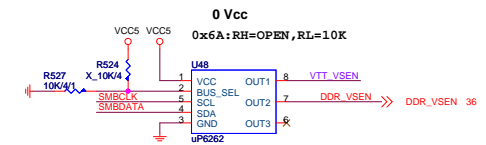
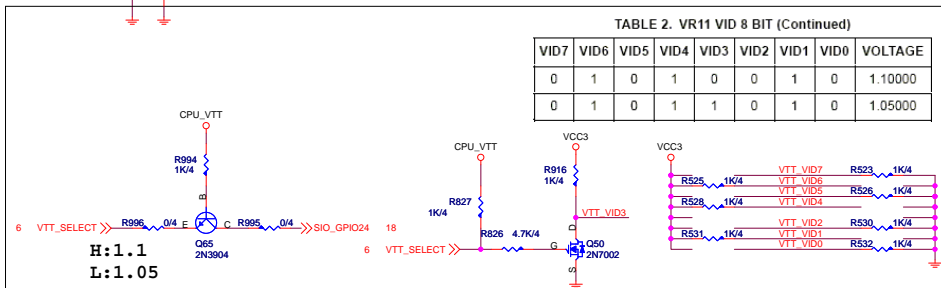
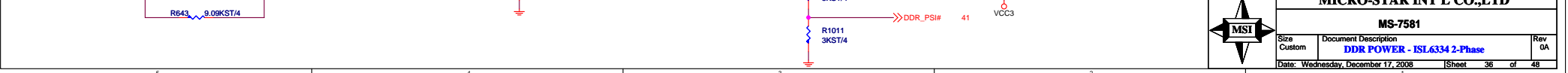
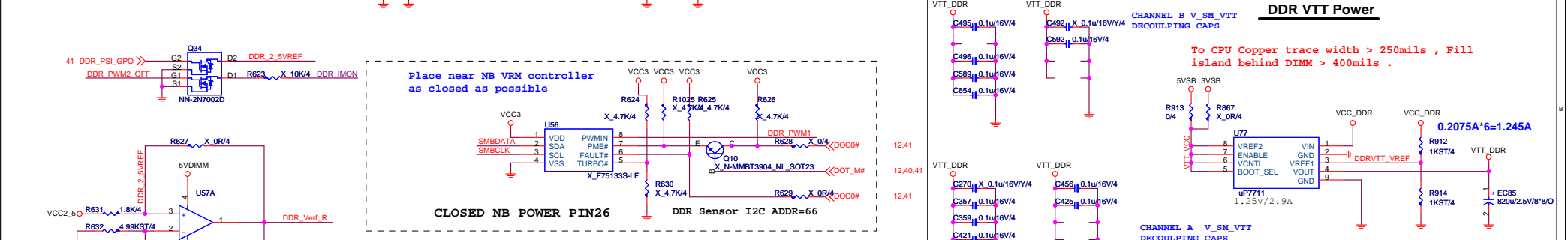


TABLE 2. VR11 VID 8 BIT

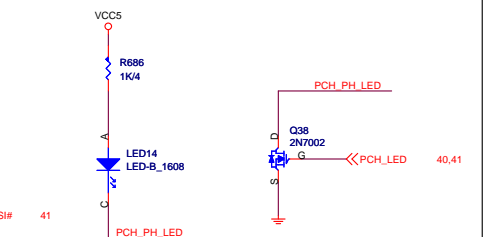
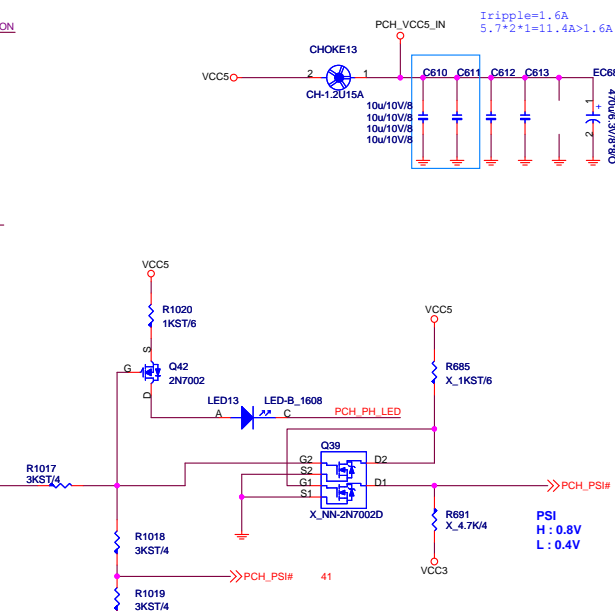
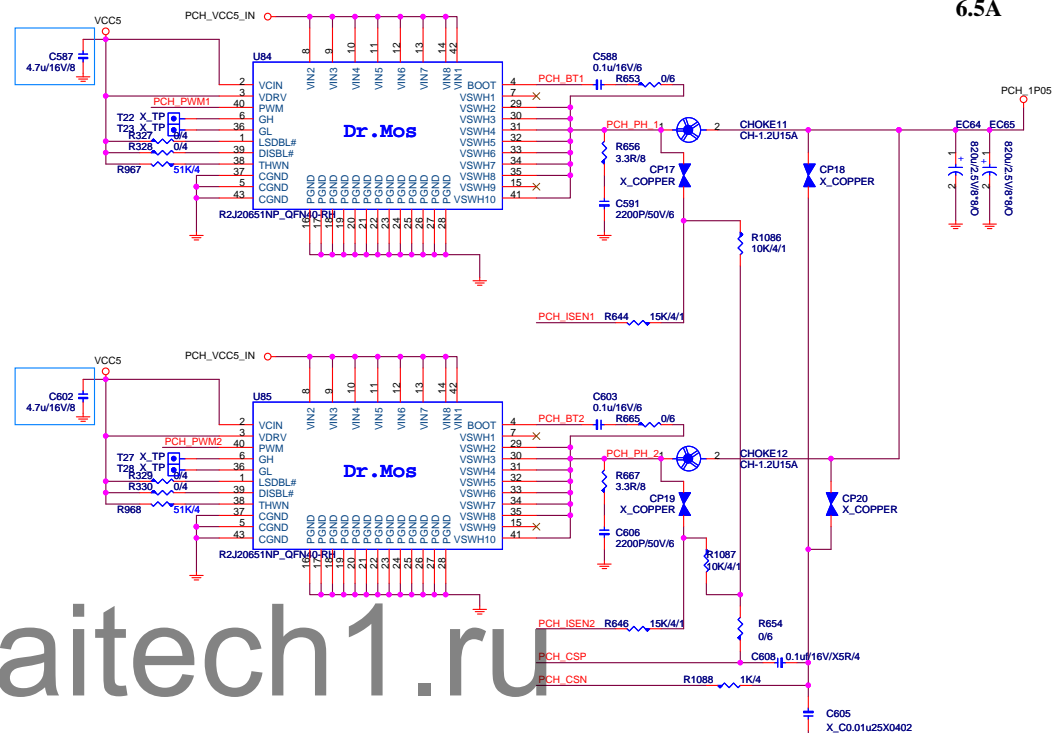
5V DIMM

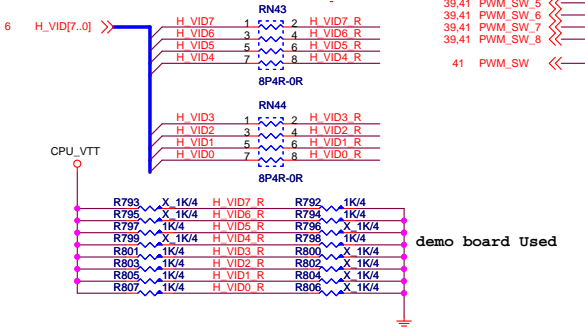
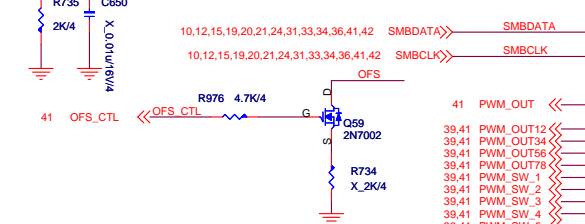
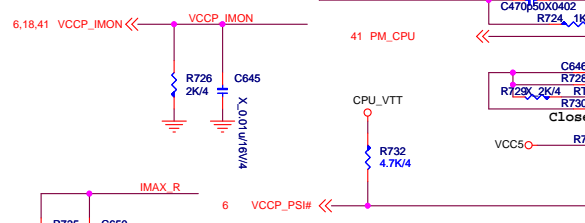
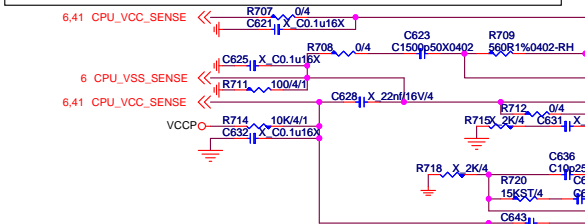
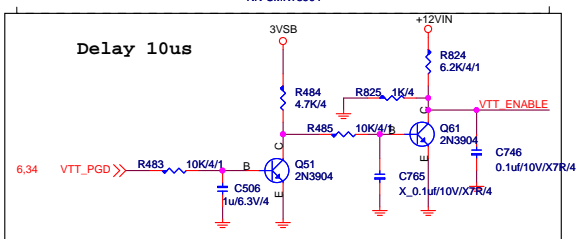
R590 1K/4 DDR_VID4
R593 1K/4 DDR_VID4

R594 1K/4 DDR_VID7
R598 1K/4 DDR_VID7
R599 1K/4 DDR_VID7
R596 1K/4 DDR_VID3
R597 1K/4 DDR_VID2
R601 1K/4 DDR_VID0

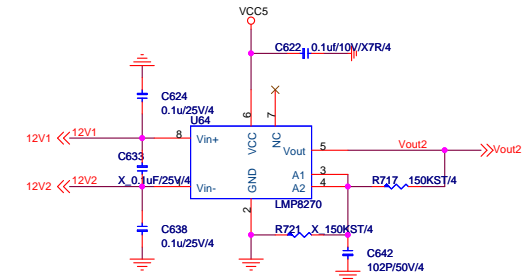
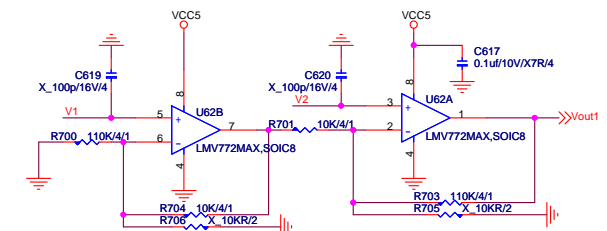


6212内部的REF(0.8V)

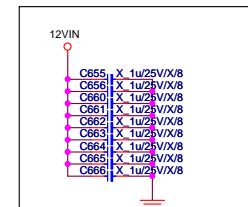




POWER WATTAGE MONITOR



V1, V2 trace length不可拉太長,
LMV772MAX放在near PWM IC



For Power team test only



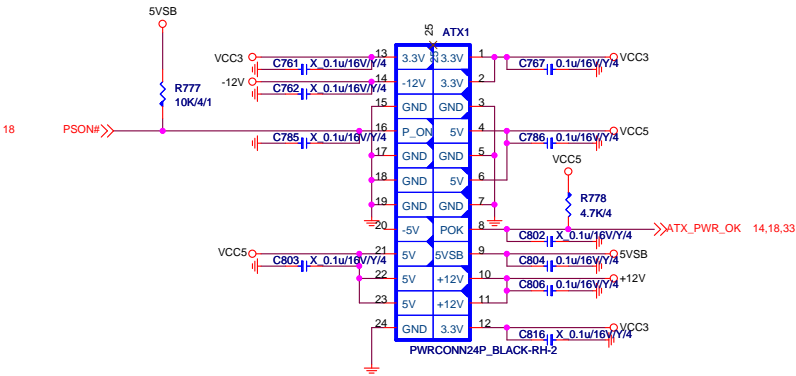
MICRO-STAR INT'L CO.,LTD

MS-7581

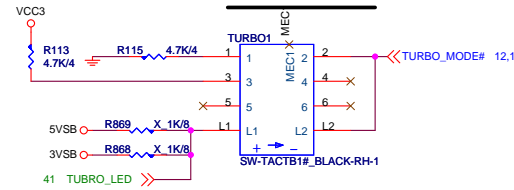
Size Custom	Document Description VRD11.1 - UP6208 8-Phase	Rev 0A
Date: Wednesday, December 17, 2008		Sheet 38 of 48



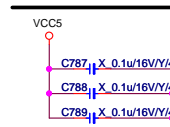
ATX POWER CONNECTOR



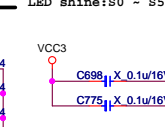
TURBO BUTTON



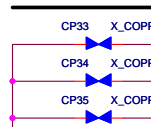
POWER ON BUTTON



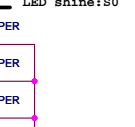
LED shine:S0 ~ S5



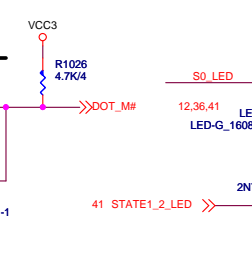
RESET BUTTON



LED shine:S0



POWER LED(S0/S3)



DEBUG LED

